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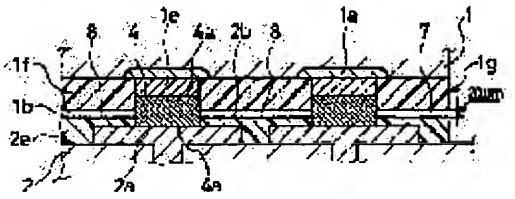
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To realize low-cost and high reliability related to a semiconductor device with flip chip connection.

SOLUTION: A chip mounting substrate 2 wherein a semiconductor chip 1 is supported by flip chip connection, a conductive member 4 which, being formed of solder paste of low melting-point solder, electrically connects a pad 1a of the semiconductor chip 1 to a land 2a of the chip mounting substrate 2, a sealing part wherein an exposed surface of the semiconductor chip 1 is covered with a sealing resin, and a solder ball which is an external terminal provided on the rear surface of the chip mounting substrate 2 are provided. The semiconductor chip 1 and the chip mounting substrate 2 are so allocated as to form a resin flow-in preventive gap part 7 which prevents flow of the sealing resin, while a gap part 8 of the same interval as the resin flow preventive gap part 7 is formed around the conductive member 4 between the chip and the substrate. further, a through hole penetrating from the gap part 8 to the outside is provided at the chip mounting



substrate 2.

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* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] while having the following, forming the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and arranging the aforementioned semiconductor chip and the aforementioned chip loading substrate -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the semiconductor device characterized by forming the gap section in the circumference of a member The chip loading substrate which is the semiconductor device which performed flip chip bonding, and supports a semiconductor chip by flip chip bonding. the conductivity in which the surface electrode of the aforementioned semiconductor chip and the substrate terminal of the aforementioned chip loading substrate were electrically connected to, and the connection with the aforementioned surface electrode and the aforementioned substrate terminal was formed with low melting point solder -- a member The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it. Two or more external terminals which were prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and were electrically connected with the aforementioned substrate terminal.
[Claim 2] while having the following, forming the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and arranging the aforementioned semiconductor chip and the aforementioned chip loading substrate -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the semiconductor device characterized by forming the gap section in the circumference of a member The chip loading substrate which is the semiconductor device which performed flip chip bonding, and supports a semiconductor chip by flip chip bonding. the conductivity which connected electrically the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate, and was formed with low melting point solder -- a member The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it. Two or more external terminals which were prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and were electrically connected with the aforementioned substrate terminal.
[Claim 3] while having the following, forming the resin inflow prevention gap section prevented in the inflow of the aforementioned resin for closure and arranging the aforementioned semiconductor chip and the aforementioned chip loading substrate -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the semiconductor device characterized by to be formed the gap section of the same interval in the circumference of a member with the aforementioned resin inflow prevention gap section The chip loading substrate which is the semiconductor device which performed flip chip bonding, and supports a semiconductor chip by flip chip bonding. the conductivity which connected electrically the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate, and was formed with low melting point solder -- a member The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it. Two or more external terminals which were prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and were electrically connected with the aforementioned substrate terminal.
[Claim 4] The semiconductor device which is characterized by providing the following and which performed flip chip bonding. The chip loading substrate which supports a semiconductor chip by flip chip bonding. the conductivity which connected electrically the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate, and was formed with low melting point solder -- a member The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it. It is prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and has two or more external terminals electrically connected with the aforementioned substrate terminal. While the aforementioned semiconductor chip and the aforementioned chip loading substrate form the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and are arranged between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the breakthrough which the gap section of the same interval is formed in the circumference of a member with the aforementioned resin inflow prevention gap section, and penetrates the aforementioned gap section and the exterior to the aforementioned chip loading substrate
[Claim 5] The manufacture method of a semiconductor device characterized by providing the following. The process which the principal plane of a semiconductor chip and the chip loading side of a chip loading substrate are made to counter, and doubles the position of the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate corresponding to this, and arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through a conductive member between the aforementioned surface electrode and the aforementioned substrate terminal. The process which fuses the aforementioned conductive member, is made to connect the aforementioned surface electrode and the aforementioned substrate terminal electrically by the aforementioned conductive member where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the

aforementioned chip loading substrate. the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity -- the process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, forming the gap section in the circumference of a member The process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.

[Claim 6] The manufacture method of a semiconductor device characterized by providing the following. The process for which the chip loading substrate in which the substrate terminal corresponding to the surface electrode of a semiconductor chip was prepared is prepared. The process which applies the soldering paste which consists of low melting point solder on the aforementioned substrate terminal of the aforementioned chip loading substrate. The process which the principal plane of the aforementioned semiconductor chip and the chip loading side of the aforementioned chip loading substrate are made to counter, and doubles the position of the aforementioned surface electrode and the aforementioned substrate terminal corresponding to this, and arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through the aforementioned soldering paste between the aforementioned surface electrode and the aforementioned substrate terminal. The aforementioned soldering paste is fused. The process which is electrically connected by the conductive member which formed the aforementioned surface electrode and the aforementioned substrate terminal from the aforementioned soldering paste where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate, the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member The process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, and the process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.

[Claim 7] The manufacture method of a semiconductor device characterized by providing the following. The process for which the chip loading substrate in which the substrate terminal corresponding to the surface electrode of a semiconductor chip was prepared is prepared. The process which applies to predetermined height the soldering paste which consists of low melting point solder on the aforementioned substrate terminal of the aforementioned chip loading substrate using height control-section material. The process which the principal plane of the aforementioned semiconductor chip and the chip loading side of the aforementioned chip loading substrate are made to counter, and doubles the position of the aforementioned surface electrode and the aforementioned substrate terminal corresponding to this, and arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through the aforementioned soldering paste between the aforementioned surface electrode and the aforementioned substrate terminal. The aforementioned soldering paste is fused. The process which is electrically connected by the conductive member which formed the aforementioned surface electrode and the aforementioned substrate terminal from the aforementioned soldering paste where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate, the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member The process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, and the process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.

[Claim 8] The manufacture method of a semiconductor device characterized by providing the following. The process which prepares the chip loading substrate by which the soldering paste of low melting point solder was beforehand applied to predetermined height on the substrate terminal corresponding to the surface electrode of a semiconductor chip. The process which the principal plane of the aforementioned semiconductor chip and the chip loading side of the aforementioned chip loading substrate are made to counter, and doubles the position of the aforementioned surface electrode and the aforementioned substrate terminal corresponding to this, and arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through the aforementioned soldering paste between the aforementioned surface electrode and the aforementioned substrate terminal. The process which fuses the aforementioned soldering paste, is electrically connected by the conductive member which formed the aforementioned surface electrode and the aforementioned substrate terminal from the aforementioned soldering paste where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate. the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- aforementioned conductivity -- the process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, forming the gap section in the circumference of a member, and the process which prepare two or more external terminals which connected with the aforementioned substrate terminal electrically in the chip loading side of the aforementioned chip loading substrate, and the field of a

[Claim 9] The manufacture method of a semiconductor device characterized by providing the following. The process for which the base substrate equipped with two or more chip loading substrates in which the substrate terminal corresponding to the surface electrode of a semiconductor chip was prepared is prepared. The process which the principal plane of two or more aforementioned semiconductor chips and the chip loading side of each aforementioned chip loading substrate of the aforementioned base substrate are made to counter, and doubles the position of the aforementioned surface electrode and the

aforementioned substrate terminal, and arranges each aforementioned semiconductor chip and the aforementioned chip loading substrate through a conductive member between the aforementioned surface electrode and the aforementioned substrate terminal. The process which fuses the aforementioned conductive member, is made to connect the aforementioned surface electrode and the aforementioned substrate terminal electrically by the aforementioned conductive member where the resin inflow prevention gap section is formed between each aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of each aforementioned semiconductor chip to each aforementioned chip loading substrate. the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between each aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member The process which is wearing the exposed surface of each aforementioned semiconductor chip with the aforementioned resin for closure, closes each semiconductor chip, and forms two or more semiconductor device book somata, The process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the process which separates each aforementioned semiconductor device book soma from the aforementioned base substrate, the chip loading side in the aforementioned chip loading substrate of each aforementioned semiconductor device book soma, and the field of an opposite side.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the semiconductor device and its manufacture method of the flip chip bonding which realizes low-cost-izing and high-reliability about a semiconductor manufacturing technology.
[0002]
[Description of the Prior Art] the technology explained below -- this invention -- research -- it faces completing, this invention person inquires, and the outline is as follows
[0003] In the semiconductor device which has the semiconductor chip in which semiconductor integrated circuits, such as memory, were formed, BGA (Ball Grid Array) is known as an example of structure which attains the miniaturization. Furthermore, in Above BGA, flip chip bonding is used as technology of attaining improvement in the speed of signal transduction.
[0004] This flip chip bonding makes the active side (principal plane) of a semiconductor chip counter with the chip loading side of a chip loading substrate, and mounts a semiconductor chip in a chip loading substrate in this state.
[0005] In addition, in case flip chip bonding of the semiconductor chip is carried out, the surface electrode of a semiconductor chip and the substrate terminal of a chip loading substrate are mainly electrically connected using conductive members, such as a bump.
[0006] In this case, with the reflow temperature at the time of mounting BGA in mounting substrates, such as a printed-circuit board, a bump's connection uses melting and the bump formed with high-melting point solder in many cases so that it may expand and a package crack (crack formed in the closure section) may not be caused.
[0007] Furthermore, in order to raise a bump's connection reliability, some which form a golden bump with big size by the galvanizing method are in the pad (surface electrode) of the aluminum of a semiconductor chip.
[0008] Here, BGA which performed flip chip bonding is indicated by JP,9-82756,A, JP,9-92685,A, JP,6-326211,A, JP,7-111278,A, and JP,9-64231,A, for example.
[0009]
[Problem(s) to be Solved by the Invention] however, in the flip chip bonding of said technology, when using high-melting point solder as a bump, you have to use the substrate which is high thermal resistance also for a chip loading substrate
[0010] Consequently, since high-melting point solder and the substrate of high thermal resistance are expensive, let it be a problem for BGA to carry out a cost rise.
[0011] Furthermore, since it is added like a plater to the manufacturing process of a semiconductor chip when forming a golden bump in the pad of a semiconductor chip by the galvanizing method, let it be a problem to introduce the facility for a plating application, consequently to lead to a cost rise like the above.
[0012] Moreover, in BGA indicated by said five official reports, in the structure, since the resin for closure is embedded to the circumference of the bump between the semiconductor chips and chip loading substrates by which flip chip bonding was carried out, melting and expanding (thermal expansion) and causing a package crack have a bump at the time of mounting of BGA.
[0013] Thereby, let it be a problem for the reliability of BGA to decrease.
[0014] The purpose of this invention is to offer the semiconductor device and its manufacture method of the flip chip bonding which realizes low-cost-izing and high-reliability.
[0015] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.
[0016]
[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0017] Namely, the chip loading substrate to which the semiconductor device of this invention supports a semiconductor chip by flip chip bonding, The conductive member in which the surface electrode of the aforementioned semiconductor chip and the substrate terminal of the aforementioned chip loading substrate were electrically connected to, and the connection with the aforementioned surface electrode and the aforementioned substrate terminal was formed with low melting point solder, The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it, It is prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and has two or more external terminals electrically connected with the aforementioned substrate terminal. while the aforementioned semiconductor chip and the aforementioned chip loading substrate form the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and are arranged -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the gap section is formed in the circumference of a member
[0018] thereby -- conductivity -- since the gap section is formed in the circumference of a member -- conductivity -- the flexibility of a member is increased -- it can make -- consequently, conductivity -- the hindrance to the thermal expansion of

a member can be reduced
[0019] therefore, the time of a conductive member carrying out thermal expansion (melting and expansion) at the time of mounting to the mounting substrate of a semiconductor device -- a conductive member -- the gap section -- it can spread -- thereby -- conductivity -- the stress generated according to the thermal expansion of a member can be made to ease
[0020] Consequently, generating of the package crack at the time of semiconductor device mounting can be prevented, and, thereby, improvement in the reliability of a semiconductor device can be aimed at.
[0021] Furthermore, the chip loading substrate to which the semiconductor device of this invention supports a semiconductor chip by flip chip bonding, The conductive member which connected electrically the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate, and was formed with low melting point solder, The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it, It is prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and has two or more external terminals electrically connected with the aforementioned substrate terminal. while the aforementioned semiconductor chip and the aforementioned chip loading substrate form the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and are arranged -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the gap section is formed in the circumference of a member
[0022] Moreover, the manufacture method of the semiconductor device of this invention makes the principal plane of a semiconductor chip, and the chip loading side of a chip loading substrate counter, and doubles the position of the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate corresponding to this. The process which arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through a conductive member between the aforementioned surface electrode and the aforementioned substrate terminal, The process which fuses the aforementioned conductive member, is made to connect the aforementioned surface electrode and the aforementioned substrate terminal electrically by the aforementioned conductive member where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate, the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member It has the process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, and the process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.
[0023] Furthermore, the process for which the chip loading substrate in which the substrate terminal corresponding to the surface electrode of a semiconductor chip in the manufacture method of the semiconductor device of this invention was prepared is prepared, The process which applies the soldering paste which consists of low melting point solder on the aforementioned substrate terminal of the aforementioned chip loading substrate, Make the principal plane of the aforementioned semiconductor chip, and the chip loading side of the aforementioned chip loading substrate counter, and the position of the aforementioned surface electrode and the aforementioned substrate terminal corresponding to this is doubled. The process which arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through the aforementioned soldering paste between the aforementioned surface electrode and the aforementioned substrate terminal, The aforementioned soldering paste is fused. The process which is electrically connected by the conductive member which formed the aforementioned surface electrode and the aforementioned substrate terminal from the aforementioned soldering paste where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate, the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member It has the process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, and the process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.
[0024]
[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing.

[0025] The perspective diagram which drawing 1 fractures a part of example of the structure of the semiconductor device (BGA) in the gestalt 1 of operation of this invention, and is shown, (Gestalt 1 of operation) Drawing 2 is drawing showing an example of the structure of BGA shown in drawing 1 . (a) A plan, The cross section with which an A-A line [in / drawing 2 (a) / (b) / a side elevation and (c), and / in drawing 3] is met, / a bottom plan view The expansion fragmentary sectional view showing the structure of the C section [in / drawing 3 / in drawing 4], the cross section with which drawing 5 meets the B-B line in drawing 2 (a), The manufacture process view showing an example of the manufacture method of a semiconductor device [in / the gestalt 1 of operation of this invention / in drawing 6] (BGA), Drawing 7 (a) and (b) The plan showing an example of the state of the base substrate in each manufacturing process of BGA shown in drawing 1 , The plan showing an example of the state of the base substrate in each manufacturing process of BGA which shows drawing 8 (a), (b), and (c) to drawing 1 , and the side elevation of BGA, Drawing 9 is the expansion fragmentary sectional view showing an example of the application state of the soldering paste in the manufacture method of BGA shown in drawing 1 . the conductivity in the manufacture method of BGA that (b) shows drawing 10 before a reflow to drawing 1 after a reflow in (a) -- the expansion fragmentary sectional view showing an example of the melting state at the time of the BGA mounting reflow of a member and drawing 11 are the physical-properties data views showing an example of the physical properties of the resin for closure used for BGA shown in drawing 1

[0026] The semiconductor device of the gestalt 1 of this operation shown in drawing 1 - drawing 5 is BGA9 in which the semiconductor chip 1 by which semiconductor integrated circuits, such as memory (for example, SSRAM (Synchronous Static Random Access Memory)), were formed in principal plane 1b was mounted in the chip loading substrate 2 by flip chip bonding, and two or more solder balls 3 were formed as an external terminal.
[0027] In addition, the gestalt 1 of this operation explains the case of BGA9 of 119 pins (7x17 pins) as an example of the above BGA 9. However, the number of external terminals, i.e., the number of installation of the solder ball 3, may not be limited to 119 pieces, and the number may be less than 119 pieces, or may be 119 or more pieces.
[0028] Moreover, in BGA9 explained with the gestalt 1 of this operation, it is arranged in the shape of a grid (7x17), and is prepared in the field (henceforth referred to as substrate rear-face 2c) of chip loading side 2b and an opposite side in which land 2a (refer to drawing 4) whose solder ball 3 is the substrate terminal of the chip loading substrate 2 as shown in drawing 2 (b) and (c) is prepared.
[0029] Therefore, as shown in drawing 3 , the signal from a semiconductor chip 1 is told to the solder ball 3 which is an external terminal through the chip loading substrate 2.
[0030] The chip loading substrate 2 which will support a semiconductor chip 1 by flip chip bonding if the composition of the above BGA 9 is explained, the conductivity which connected electrically pad 1a (surface electrode) of a semiconductor chip 1, and land 2a of the chip loading substrate 2, and was formed with low melting point solder -- with a member 4 The closure section 6 which was wearing tooth-back 1c (exposed surface) of a semiconductor chip 1, and 1d (exposed surface) of sides with the resin 5 for closure, and formed them, Plurality which was prepared in substrate rear-face 2c of the chip loading substrate 2, and was electrically connected with land 2a (here) While it consists of 119 solder balls 3 which are external terminals, and a semiconductor chip 1 and the chip loading substrate 2 form the resin inflow prevention gap section 7 which prevents the inflow of the resin 5 for closure and are arranged between a semiconductor chip 1 and the chip loading substrates 2 (it omits between a chip-substrate henceforth) -- setting -- conductivity -- 2d of breakthroughs which the gap section 8 of the same interval is formed in the circumference of a member 4 with the resin inflow prevention gap section 7, and penetrate the gap section 8 and the exterior to the chip loading substrate 2 is prepared
[0031] 2d of this breakthrough is a vent hole for missing outside the gas which occurs in the gap section 8 at the time of a mould and a reflow etc.
[0032] Moreover, a semiconductor chip 1 is mounted in chip loading side 2b of the chip loading substrate 2 by flip chip bonding while it is formed with silicon.
[0033] in addition, as shown in drawing 1 , flip chip bonding is effective connection technology, when the size of a semiconductor chip 1 is comparatively large and it shortens connection distance between chip-substrates by this to the size of the appearance of BGA9 at the well of the case where application of wirebonding technology is difficult, and improvement in the speed of signal transduction
[0034] Drawing 4 is drawing having expanded and shown the structure of the flip-chip-bonding section of the gestalt 1 of this operation. Flip chip bonding makes the active side (principal plane 1b) of a semiconductor chip 1 counter with chip loading side 2b of the chip loading substrate 2, and mounts a semiconductor chip 1 in the chip loading substrate 2 in this state (face down).
[0035] in addition, pad 1a of a semiconductor chip 1 is formed by aluminum -- having -- a semiconductor chip 1 -- setting -- the upper layer of pad 1a -- conductivity -- barrier metal layer 1e electrically connected with connection 4a of a member 4 and 1f of protective coats which protect pad 1a are formed In that case, barrier metal layer 1e is formed of for example, a palladium-titanium alloy or a nickel chromium alloy, and exposes the front face, and is surrounded by 1f of protective coats, and, on the other hand, 1f of protective coats is formed of the insulator layer of for example, a polyimide system.
[0036] Furthermore, land 2a of the chip loading substrate 2 is formed for example, of the golden-copper alloy.
[0037] the conductivity which pad 1a of a semiconductor chip 1 and land 2a of the chip loading substrate 2 corresponding to this become from low melting point solder with the gestalt 1 of this operation here -- it connects directly electrically through the member 4 That is, it is the flip chip bonding by the eutectic-solder connection using low melting point solder.
[0038] In addition, the aforementioned low melting point solder is fused by the reflow at the temperature of 250 degrees C or less, and is low-temperature solder which is the grade which can be soldered.
[0039] Moreover, in case the aforementioned flip chip bonding is performed, thereby, a reflow of the soldering paste 10 (refer to drawing 9) applied to predetermined height by printing is carried out to land 2a of the chip loading substrate 2, or pad 1a of a semiconductor chip 1, the aforementioned soldering paste 10 is fused at once, it is made to harden and flip chip bonding is performed after that.
[0040] Consequently, the resin inflow prevention gap section 7 of an almost uniform request distance is formed over the whole periphery between chip-substrates.
[0041] This resin inflow prevention gap section 7 is the crevice formed so that the resin 5 for closure might not enter between chip-substrates at the time of a resin seal, and is formed in the grade which can prevent the inflow of the resin 5 for closure at the time of a resin seal very narrowly.
[0042] Moreover, the closure section 6 of BGA9 of the gestalt 1 of this operation is formed of the transfermold which used the resin 5 for closure among resin seals.
[0043] Therefore, the set point of the distance of the aforementioned resin inflow prevention gap section 7 is determined by the physical properties of the resin 5 for closure used with the gestalt 1 of this operation shown in drawing 11 , and the mould conditions at the time of the mould mentioned later, and, in the case of the gestalt 1 of this operation, the distance of the resin inflow prevention gap section 7 is about 20 micrometers as the example.
[0044] However, if the value of the distance of the resin inflow prevention gap section 7 is the size which can prevent the inflow of a between [the chip-substrates of the resin 5 for closure at the time of a resin seal], it is not limited to 20 micrometers and can be variously changed according to combination, its kind, etc. of the resin 5 (for example, fluidity) for closure to be used, and mould conditions at the time of a mould.
[0045] In addition, since the resin 5 for closure does not flow between chip-substrates in the above BGA 9 as described above, in case the resin seal of the semiconductor chip 1 is carried out by the mould method, each conductivity which consists of low melting point solder -- the gap section 8 is formed in the circumference of a member 4, and the resin inflow

prevention gap section 7 formed over the whole periphery between chip-substrates and the gap section 8 of the inner direction between chip-substrates are formed in the same distance in BGA9 of the gestalt 1 of this operation
[0046] That is, principal plane 1b of a semiconductor chip 1 and chip loading side 2b of the chip loading substrate 2 are mutually formed of a flat field, and thereby, it is formed so that the distance between chip-substrates may be mostly set to about 20 micrometers from 1g of periphery sections of a semiconductor chip 1 over the whole inner one at homogeneity.
[0047] moreover, between a chip-substrate -- setting -- each conductivity -- a semiconductor chip 1 can consider curving slightly in the sense by which the circuit forming face (principal plane 1b) is pulled by having formed the gap section 8 in the circumference of a member 4 This amount of curvatures of a semiconductor chip 1 must be the amount of curvatures of the grade which does not form a crack in principal plane 1b of a semiconductor chip 1 in that case.
[0048] In the gap section 8 during installation of a member 4 therefore, two or more conductivity which supports a semiconductor chip 1 -- the conductivity which adjoins among members 4 -- two conductivity from which the installation pitch of a member 4 serves as the maximum -- Having to consider the size of the gap section 8 as it being possible to stop in the amount of curvatures of the grade which does not form a crack in the principal plane 1b, when a semiconductor chip 1 curves, the 20-micrometer gap section 8 in the gestalt 1 of this operation satisfies this condition.
[0049] Moreover, using the resin 5 for closure, the closure section 6 of the above BGA 9 closes a semiconductor chip 1 by transfermold, and is formed, and as shown in drawing 1 and drawing 2 (a), the resin 5 for closure near the circumference of a semiconductor chip 1 in the chip loading substrate 2 are joined over the perimeter almost in accordance with 1d of four sides of a semiconductor chip 1.
[0050] In addition, the resin 5 for closure shows the physical properties of the resin 5 for closure used in the gestalt 1 of this operation as the example to drawing 11 , although it is a thermosetting epoxy system resin etc.
[0051] Moreover, the chip loading substrate 2 is a printed-circuit board of plastics with the comparatively cheap and moderate thermal resistance (not a high heatproof but thermal resistance for example, around 300 degrees C) formed using for example, the epoxy system resin containing glass, the bismaleimide triazine containing glass (BT resin containing glass), etc.
[0052] Therefore, BGA9 of the gestalt 1 of this operation is called P-BGA (plastics BGA).
[0053] Moreover, as shown in drawing 3 , the chip loading substrate 2 is a substrate of the multilayer-interconnection structure where 2f of front wiring and 2g of internal wiring were formed, while the front face is coated with solder-resist 2e, as shown in drawing 5 . The chip loading substrate 2 of the gestalt 1 of this operation is a substrate of four layer structures with four wiring layers in 2f of front wiring of chip loading side 2b, the front wiring of 2f of substrate rear-face 2c, and 2g of two internal wiring, as shown in drawing 3 .
[0054] However, the chip loading substrate 2 is not limited to the substrate of four layer structures.
[0055] Furthermore, 2d of one breakthrough of a vent-hole function is formed in the part which avoided land 2a near the center of chip loading side 2b. However, also about the number of installation of 2d of breakthroughs, it may not be limited and more than one may be prepared.
[0056] moreover, the solder ball 3 which is the external terminal of BGA9 -- conductivity -- it is formed with low melting point solder like a member 4, and the size is about 0.75mm in diameter
[0057] Next, the manufacture method of the semiconductor device (BGA) by the gestalt 1 of this operation is explained.
[0058] In addition, the manufacture method of the aforementioned semiconductor device is two or more sheets (here, although the case of six sheets is explained as the example) which are the manufacture methods of BGA9 shown in drawing 1 - drawing 5 , and are shown in drawing 7 and drawing 8 with the gestalt 1 of this operation. Based on the manufacture process which shows the case where BGA9 of plurality (six pieces) is manufactured to drawing 6 , it explains from one base substrate 11 equipped with chip loading substrates 2 of being two or more sheets other than six sheet.
[0059] First, by Step S1 shown in drawing 6 , the dicing which prepares a semiconductor wafer (not shown) equipped with two or more semiconductor chips 1 in which the desired semiconductor integrated circuit was formed, then is shown in Step S2 is performed, and the aforementioned semiconductor wafer is cut and separated at each semiconductor chip 1.
[0060] Then, the semiconductor chip 1 judged by inspection etc. to be an excellent article is prepared, and the base substrate 11 further equipped with six chip loading substrates 2 in which substrate terminal 2a corresponding to pad 1a of this semiconductor chip 1 was prepared is prepared.
[0061] Here, the base substrate 11 is a large-sized substrate which arranged the aforementioned BGA field in one train continuously while forming six pieces of the chip loading substrate 2 equivalent to one BGA field in one, as shown in drawing 7 (a).
[0062] Moreover, two or more tooling-holes 11a and guide long hole 11b which are used for this base substrate 11 at the time of a mould or cutting etc. are respectively prepared in the both-sides section along with the longitudinal direction of the base substrate 11 corresponding to each chip loading substrate 2.
[0063] That is, the base substrate 11 is a substrate which took and **(ed) six chip loading substrates 2.
[0064] Then, while performing base substrate supply shown in Step S3, soldering paste supply shown in step S4 is performed, and soldering paste printing shown in Step S5 to substrate terminal 2a of each chip loading substrate 2 of the base substrate 11 is performed.
[0065] the soldering paste 10 which consists of low melting point solder shown in drawing 9 (a) with the gestalt 1 of this operation here in case the aforementioned soldering paste printing is performed -- a mask -- it carries out to predetermined height by carrying out a printing application on substrate terminal 2a of the chip loading substrate 2 using a member 12 (height control-section material)
[0066] in addition, a mask -- a member 12 is a member for carrying out the printing application of the soldering paste 10 at height highly precise on substrate terminal 2a
[0067] With the gestalt 1 of this operation, the resin inflow prevention gap section 7 and the gap section 8 are formed in about 20 micrometers. as an example of a method which realizes this -- a mask -- the time of forming the soldering paste 10 of low melting point solder on substrate terminal 2a by the member 12 -- the diameter of 40 micrometers -- and soldering paste 10 is formed with a precision sufficient to a cylindrical shape with a height of 100 micrometers
[0068] namely, the diameter of 40 micrometers -- and the soldering paste 10 of a cylindrical shape with a height of 100

micrometers -- it should form -- opening -- a mask -- it is formed in the member 12
[0069] If the soldering paste 10 in which this height and size were controlled with high precision, and were formed on substrate terminal 2a is fused by the reflow and stiffened after that, as shown in drawing 9 (b), the resin inflow prevention gap section 7 and the gap section 8 can be formed in about 20 micrometers.
[0070] In addition, the connection reliability between chip-substrates can be improved by making the printing (application) height of soldering paste 10 as low as possible. However, the size or configuration of soldering paste 10 which are printed on substrate terminal 2a are not determined by the distance of the resin inflow prevention gap section 7 and the gap section 8 etc., and neither the aforementioned size nor a configuration (the gestalt 1 of this operation the diameter of 40 micrometers and cylindrical shape with a height of 100 micrometers) is limited to this in that case.
[0071] a mask -- on the base substrate 11 by the aforementioned printing method using the member 12, after carrying out the printing application of the soldering paste 10 on predetermined substrate terminal 2a of the chip loading substrate 2 at predetermined height Principal plane 1b of six semiconductor chips 1 and chip loading side 2b of the chip loading substrate 2 corresponding to each are made to counter. And the position of pad 1a of each semiconductor chip 1 and substrate terminal 2a corresponding to this is doubled, and a semiconductor chip 1 and the chip loading substrate 2 are further arranged through soldering paste 10 between pad 1a and substrate terminal 2a.
[0072] That is, chip mounting shown in Step S6 using the chip mounter for the existing flip chip bonding etc. is performed.
[0073] The base substrate 11 shown in drawing 7 (b) shows the state where chip mounting of the six semiconductor chips 1 was carried out to each BGA field.
[0074] Then, through and this perform the reflow shown in Step S7 at the reflow furnace which does not illustrate the base substrate [finishing / chip mounting] 11 shown in drawing 7 (b).
[0075] That is, by the aforementioned reflow, soldering paste 10 is fused and, thereby, between a chip-substrate is connected electrically.
[0076] consequently, the conductivity which formed pad 1a and substrate terminal 2a from soldering paste 10 where the resin inflow prevention gap section 7 is formed between six semiconductor chips 1 and the chip loading substrate 2 corresponding to these -- by the member 4, it can be made to connect electrically and, thereby, flip chip bonding of each semiconductor chip 1 is carried out to each chip loading substrate 2
[0077] In addition, the reflow temperature at the time of a reflow is 240-250 degrees C.
[0078] Here, soldering paste 10 is the height and size (here). Since a cylindrical shape with a diameter [of 40 micrometers] and a height of 100 micrometers is controlled with high precision and applied, the aforementioned reflow -- soldering paste 10 -- once -- fusing -- after that -- getting cold -- hardening -- conductivity -- if it becomes a member 4, as shown in drawing 4 and drawing 9 (b), the distance of the distance 7 of a semiconductor chip 1 and the chip loading substrate 2, i.e., the resin inflow prevention gap section, and the gap section 8 will be set to 20 micrometers
[0079] Resin supply for closure which supplies this is performed after a reflow end using the resin 5 for closure of the physical properties shown in drawing 11 (Step S8), and the resin seal of a semiconductor chip 1 is performed (step S9).
[0080] In addition, in the gestalt 1 of this operation, transfermold performs a resin seal.
[0081] Moreover, with the gestalt 1 of this operation, the mould conditions at the time of performing a mould, the physical properties of the resin 5 for closure, and the distance of the resin inflow prevention gap section 7 become an important factor for not making the resin 5 for closure permeate between chip-substrates at the time of a mould.
[0082] Then, when the distance of the resin inflow prevention gap section 7 is set up with about 20 micrometers, while the resin 5 for closure which cannot permeate between chip-substrates is a resin which has the physical properties shown in drawing 11 , the mould conditions for not making the resin 5 for closure permeate between chip-substrates at the time of a mould are the things of the following content.
[0083] the mould which does not illustrate the aforementioned mould conditions -- metal mold -- the plunger pressure which is a pressure when extruding the resin 5 for closure inside -- 150 kg/cm2 and a mould -- in MAX, the speed [t / 50] at which the clamp pressure (mold-clamp pressure) of metal mold flows, and 175 degrees C and the resin 5 for closure flow / a die temperature / is 1.62 mm/sec, and mould time is 220 seconds
[0084] Therefore, if the aforementioned mould conditions perform transfermold, using the resin 5 for closure which has the physical properties shown in drawing 11 in order that the 20-micrometer resin inflow prevention gap section 7 may prevent the inflow of a between [the chip-substrates of the resin 5 for closure] and the resin 5 for closure may not permeate between chip-substrates by this -- between each semiconductor chip 1 and the chip loading substrates 2 -- conductivity -- the gap section 8 can be formed in the circumference of a member 4
[0085] consequently, between a chip-substrate -- conductivity -- with the structure which formed the gap section 8 in the circumference of a member 4, tooth-back 1c of each semiconductor chip 1 and 1d of sides are worn with the resin 5 for closure, six semiconductor chips 1 are boiled, respectively, are closed, and the closure section 6 is formed
[0086] In addition, in the resin seal of the gestalt 1 of this operation, the resin 5 for closure is supplied to the exposed surface of a semiconductor chip 1, i.e., tooth-back 1c, and 1d of sides, a semiconductor chip 1 is completely covered with the resin 5 for closure on the chip loading substrate 2, and the closure section 6 is formed.
[0087] This forms BGA book soma 9a (semiconductor device book soma) containing the six closure sections 6 on one base substrate 11, as shown in drawing 8 (a).
[0088] Then, six BGA book soma 9a is cut, respectively, and it is made to dissociate from the base substrate 11, as shown in drawing 8 (b) (Step S10).
[0089] As a cutting process in that case, a router (drill) may be used and mold cutting etc. may cut.
[0090] Then, the solder ball 3 which is the external terminal of plurality (the gestalt 1 of this operation 119 pieces) electrically connected with substrate terminal 2a, and is set to the field of chip loading side 2b and an opposite side, i.e., substrate rear-face 2c, in the chip loading substrate 2 of each BGA book soma 9a from low melting point solder is formed.
[0091] Here, first, solder ball supply (Step S11) is performed, the solder ball imprint shown in Step S12 is performed further, and temporary fixation of the 119 solder balls 3 is carried out at the chip loading substrate 2 of each BGA book soma 9a.
[0092] Then, through and this perform the reflow shown in Step S13 at the reflow furnace which does not illustrate the base substrate 11 which carried out temporary fixation of the solder ball 3 to each chip loading substrate 2.

[0093] That is, the solder ball 3 is attached in the chip loading substrate 2 by the reflow shown in Step S13.
[0094] In addition, the reflow temperature at the time of a reflow is 240-250 degrees C.
[0095] here -- conductivity -- since a member 4 is formed from the soldering paste 10 of low melting point solder, it is shown in drawing 10 at the time of a 240-250-degree C reflow -- as -- each conductivity -- it fuses, and a member 4 expands thermally and spreads in a longitudinal direction
[0096] this time -- BGA9 of the gestalt 1 of this operation -- each conductivity -- since the gap section 8 is formed in the circumference of a member 4 -- conductivity -- the increase of flexibility, consequently conductivity of a member 4 -- a member 4 can be spread and shortened in the gap section 8
[0097] Thereby, the solder ball 3 which is the external terminal which consists of low melting point solder is attached.
[0098] Consequently, BGA9 as shown in drawing 1 or drawing 8 (c) can be manufactured, and, thereby, it can consider as BGA completion (Step S14).
[0099] According to the semiconductor device (BGA) and its manufacture method of a gestalt 1 of this operation, the following operation effects are acquired.
[0100] That is, the inflow of the resin 5 for closure of a between [the chip-substrate at the time of a mould (at the time of a resin seal)] can be prevented by a semiconductor chip 1 and the chip loading substrate 2 forming the resin inflow prevention gap section 7, and arranging them.
[0101] therefore, between the aforementioned chip-substrate -- setting -- conductivity -- the gap section 8 can be formed in the circumference of a member 4
[0102] thereby -- conductivity -- since the gap section 8 is formed in the circumference of a member 4 -- conductivity -- the flexibility of a member 4 is increased -- it can make -- consequently, conductivity -- the hindrance to the thermal expansion and cooling of a member 4 can be reduced
[0103] therefore, the time of mounting to mounting substrates, such as a printed circuit board of the time of the solder ball 3 (external terminal) installation by the reflow, or BGA9, -- conductivity -- the time of a member 4 carrying out thermal expansion (melting and expansion) -- conductivity -- a member 4 can spread in the gap section 8, and it can also be shortened when it got cold and hardens
[0104] thereby -- conductivity -- the stress generated according to the thermal expansion (cooling) of a member 4 can be made to ease
[0105] Consequently, generating of the package crack at the time of BGA9 mounting can be prevented, and, thereby, improvement in the reliability of BGA9 can be aimed at.
[0106] Furthermore, it can also be prevented the connectability between chip-substrates deteriorating.
[0107] moreover, the time of BGA9 mounting -- conductivity -- since a member 4 can expand thermally and it can spread in the gap section 8 -- conductivity -- melting of a member 4 -- being permissible -- consequently, conductivity -- it becomes possible to use low melting point solder for a member 4
[0108] therefore, the thing for which a printed-circuit board with the thermal resistance which it is comparatively cheap and is not a high heatproof is used to the chip loading substrate 2 -- possible -- becoming -- conductivity -- low-cost-ization of BGA9 can be attained together with using low melting point solder for a member 4
[0109] moreover, between a chip-substrate -- setting -- conductivity -- since this gap section 8 is about about 20 micrometers by forming the gap section 8 of the same interval in the circumference of a member 4 with the resin inflow prevention gap section 7, when a big load is applied to a semiconductor chip 1 at the time of a mould, it can prevent that curvature which forms a crack in principal plane 1b of a semiconductor chip 1 occurs
[0110] Thereby, improvement in the reliability of BGA9 can be aimed at.
[0111] Furthermore, the gas which occurs in the gap section 8 at the time of the elevated-temperature addition at the time of a mould and BGA9 mounting etc. can be missed outside through 2d of breakthroughs by preparing 2d of breakthroughs which penetrate the gap section 8 and the exterior to the chip loading substrate 2.
[0112] Thereby, generating of the package crack in BGA9 can be reduced further.
[0113] Moreover, since principal plane 1b and tooth-back 1c of a semiconductor chip 1 are not exposed by wearing tooth-back 1c and 1d of sides which are an exposed surface of a semiconductor chip 1 with the resin 5 for closure, and forming the closure section 6, touching tooth-back 1c of a semiconductor chip 1 directly at the time of the characterization of BGA9 and mounting etc. is lost.
[0114] Since it can reduce by this that external force is added to a semiconductor chip 1, generating of the faulty connection between a chip crack or a chip-substrate can be prevented.
[0115] Consequently, improvement in the reliability of BGA9 can be aimed at.
[0116] Furthermore, since the handling of BGA9 becomes easy by carrying out the resin seal of the semiconductor chip 1, the manufacturability can be improved.
[0117] Moreover, by applying the soldering paste 10 of low melting point solder on substrate terminal 2a of the chip loading substrate 2, in a last process (manufacturing process of a semiconductor chip 1), the process which forms a solder bump on pad 1a of a semiconductor chip 1 can be deleted, and it becomes possible to consider as the same last process as the semiconductor chip 1 which does not perform flip chip bonding by this.
[0118] Therefore, since the facility only for bump formation for performing flip chip bonding of BGA9 of the gestalt 1 of this operation becomes unnecessary consequently, low-cost-ization of BGA9 can be attained.
[0119] Moreover, by manufacturing BGA9 using the base substrate 11 equipped with six chip loading substrates 2, it becomes possible to manufacture six BGA9 simultaneously from one base substrate 11, and, thereby, BGA9 can be manufactured efficiently. That is, the throughput in the manufacturing process of BGA9 can be improved.
[0120] Consequently, the manufacturability of BGA9 can be improved.
[0121] (Gestalt 2 of operation) the conductivity prepared in the semiconductor chip of BGA which shows the cross section showing an example of the structure of a semiconductor device [in / the gestalt 2 of operation of this invention / in drawing 12] (BGA), the expansion fragmentary sectional view showing the structure of the D section / in / drawing 12 / in drawing 13], and drawing 14 to drawing 12 -- it is the bottom plan view showing an example of the array of a member
[0122] Although BGA20 (semiconductor device) shown in drawing 12 in the gestalt 2 of this operation mounts a

semiconductor chip 1 in the chip loading substrate 2 by flip chip bonding like BGA9 explained with the gestalt 1 of operation and it has the almost same structure as BGA9 The change part over BGA9 of the gestalt 1 of operation it is shown in drawing 13 -- as -- conductivity -- it is with using the small solder ball which becomes a member 4 from low melting point solder, and forming only in the part corresponding to 1g of periphery sections of the semiconductor chip 1 of the chip loading substrate 2 the resin inflow prevention gap section 7 which prevents the inflow of the resin 5 for closure
[0123] therefore, BGA20 -- the conductivity of the aforementioned small solder ball -- flip chip bonding of the semiconductor chip 1 is carried out to the chip loading substrate 2 through a member 4
[0124] the gestalt 2 of this operation here -- conductivity -- the size of the aforementioned small solder ball used as a member 4 is about 0.2mm in diameter
[0125] Thereby, when flip chip bonding of the semiconductor chip 1 is carried out to the chip loading substrate 2 by the reflow etc., the distance of the gap section 8 between chip-substrates turns into distance of a grade [a little] shorter than 0.2mm.
[0126] Therefore, the 20-micrometer resin inflow prevention gap section 7 is formed only in the part corresponding to 1g of periphery sections of the semiconductor chip 1 of the chip loading substrate 2 at the time of carrying a semiconductor chip 1 in the chip loading substrate 2.
[0127] That is, as shown in drawing 13 , 2h of dam sections of the letter of a salient which consists of solder-resist 2e is prepared in the part corresponding to Tg perimeter of periphery sections of the semiconductor chip 1 of the chip loading substrate 2, and this realizes formation of the 20-micrometer resin inflow prevention gap section 7.
[0128] the conductivity of the small solder ball of the gestalt 2 of this operation here -- in case a member 4 performs flip chip bonding, beforehand, it is carried in the pad 1a side of a semiconductor chip 1, and a face down carries out flip chip mounting (chip mounting) of the semiconductor chip 1 which carried this small solder ball to the chip loading substrate 2
[0129] In addition, the distance of the gap section 8 in BGA20 of the gestalt 2 of this operation is the distance of a grade short a little, and is longer than 0.2mm to ** compared with 20 micrometers of BGA9 of the gestalt 1 of operation.
[0130] Therefore, in case transfermold performs a resin seal, we are anxious about a semiconductor chip 1 curving according to a mould load, and being divided.
[0131] however, by BGA20 of the gestalt 2 of this operation, in order to reduce the curvature of the semiconductor chip 1 at the time of a mould, it is shown in drawing 14 -- as -- the conductivity of the small solder ball of plurality (here about 140 pieces) -- the member 4 is attached in the semiconductor chip 1 in the grid-like array
[0132] In addition, in case the aforementioned grid-like array is performed, when the number of the aforementioned small solder balls is insufficient, the dummy bump who is not making electric connection between chip-substrates is attached, and a grid-like array is prepared.
[0133] Since it is the same as that of BGA9 explained with the gestalt 1 of operation about the structure of others in BGA20 of the gestalt 2 of this operation here, the duplication explanation is omitted.
[0134] Moreover, although the manufacture method of BGA20 of the gestalt 2 this operation is almost the same as the manufacture method of BGA9 of the gestalt 1 operation The difference with the gestalt 1 of operation in BGA9 of the gestalt 1 of operation As opposed to having applied soldering paste 10 to the chip loading substrate 2 side, and having performed flip chip bonding in BGA20 of the gestalt 2 of this operation the conductivity which consists of low melting point solder using stud bump technology (bump junction technology in which ball bonding was used) etc. -- it is forming the small solder ball of a member 4 in the pad 1a side of a semiconductor chip 1, and performing flip chip bonding after that
[0135] About the manufacture method of others in the manufacture method of BGA20 of the form 2 this operation, since it is the same as that of BGA9 explained with the form 1 of operation, the duplication explanation is omitted.
[0136] Furthermore, about the operation effect acquired by BGA20 and its manufacture method of a form 2 of this operation, since it is the same as that of the basis of BGA9 explained with the form 1 of operation, the duplication explanation is omitted.
[0137] As mentioned above, although invention made by this invention person was concretely explained based on the form of implementation of invention, it cannot be overemphasized by this invention that it can change variously in the range which is not limited to the form of implementation of the aforementioned invention and does not deviate from the summary.
[0138] For example, with the form 1 of the aforementioned implementation, in case flip chip bonding is performed, the chip loading substrate 2 in which substrate terminal 2a corresponding to pad 1a of a semiconductor chip 1 was prepared is prepared. furthermore, the soldering paste 10 which consists of low melting point solder -- a mask, although the case where flip chip bonding was performed was explained after carrying out a printing application on substrate terminal 2a of the chip loading substrate 2 at predetermined height using a member 12 The soldering paste 10 which consists of low melting point solder on substrate terminal 2a corresponding to pad 1a of a semiconductor chip 1 may prepare the chip loading substrate 2 beforehand applied to predetermined height, and may perform flip chip bonding after that.
[0139] The process which carries out the printing application of the soldering paste 10 which consists of low melting point solder on substrate terminal 2a of the chip loading substrate 2 by this at predetermined height can be deleted, and the manufacturing process of a semiconductor device can be simplified.
[0140] moreover -- the form 1 of the aforementioned implementation, and the form 2 of the aforementioned implementation -- conductivity, although the case where a member 4 was formed from the soldering paste 10 or the small solder ball of low melting point solder was explained conductivity -- the whole forms a member 4 from low melting point solder -- it is not necessary to have -- conductivity -- it can set to a member 4 -- connection 4a by the side of pad 1a of a semiconductor chip 1 and connection 4a by the side of substrate terminal 2a of the chip loading substrate 2 should just be formed with low melting point solder at least
[0141] Furthermore, in the form 1 of the aforementioned implementation, although the case where the soldering paste 10 which consists of low melting point solder was applied to the substrate terminal 2a side of the chip loading substrate 2 was explained, you may apply and carry out flip chip bonding of the soldering paste 10 to the pad 1a side of a semiconductor chip 1.
[0142] moreover, the conductivity attached in a semiconductor chip 1 in the form 2 of the aforementioned implementation -- although the case where the array of the small solder ball which is a member 4 was a grid-like array was explained, the array

of the soldering paste 10 in the semiconductor chip 1 of the form 1 of the aforementioned implementation may be a grid-like array, and may be arrays other than a grid-like array
[0143] However, when the mould load applied to a semiconductor chip 1 at the time of a mould is taken into consideration, as for the array of soldering paste 10, also in the form 1 of the aforementioned implementation, it is desirable that it is a grid-like array.
[0144] Moreover, although the form 1 of the aforementioned implementation and the form 2 of the aforementioned implementation explained the case where the semiconductor device (BGA) of plurality (six pieces) was manufactured from one base substrate 11 Also in the form 1 of the aforementioned implementation, and the form 2 of the aforementioned implementation, the chip loading substrate 2 by which cutting separation was carried out may be beforehand prepared for one BGA, and BGA9 or BGA20 may be manufactured using this chip loading substrate 2.
[0145] Furthermore, although the case where a resin seal was carried out by the transfermold method was explained with the gestalt 1 of the aforementioned implementation, and the gestalt 2 of the aforementioned implementation when performing a resin seal, you may perform the aforementioned resin seal by the potting method etc.
[0146] Moreover, although the form 1 of the aforementioned implementation and the form 2 of the aforementioned implementation explained the case where a heat-resistant low printed-circuit board was comparatively used as a chip loading substrate 2, you may use the ceramic substrate of high thermal resistance etc. for the chip loading substrate 2.
[0147] That is, although the semiconductor device in the form 1 of the aforementioned implementation and the form 2 of the aforementioned implementation was P(plastics)-BGA, the aforementioned semiconductor device may be C(ceramic)-BGA.
[0148] Furthermore, the aforementioned semiconductor device is P-PGA (Pin Grid Array) which used not the solder ball 3 but the pin member for the external terminal. You may be C-PGA etc.
[0149] Moreover, the aforementioned semiconductor device may carry out the resin seal of not only a thing but the microcomputer and the semiconductor chip 1 of a logic function which carry out the resin seal of the semiconductor chip 1 of memory.
[0150]
[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0151] (1) . semiconductor chip and a chip loading substrate form the resin inflow prevention gap section, and are arranged -- between a chip-substrate -- setting -- conductivity -- the gap section can be formed in the circumference of a member Thereby, when a conductive member tends to expand thermally at the time of the external terminal installation by the reflow, or mounting to the mounting substrate of a semiconductor device, a conductive member can spread in the gap section. therefore, conductivity -- the stress generated according to the thermal expansion of a member can be made to be able to ease, consequently generating of the package crack at the time of semiconductor device mounting can be prevented Thereby, improvement in the reliability of a semiconductor device can be aimed at.
[0152] (2) Since generating of the package crack of . semiconductor device can be prevented, it can also be prevented the connectability between chip-substrates deteriorating.
[0153] (3) -- since a conductive member can expand thermally at the time of . semiconductor device mounting and it can spread in the gap section -- conductivity -- it becomes possible to be able to permit melting of a member, consequently to use low melting point solder for a conductive member Therefore, it becomes possible to use a comparatively cheap printed-circuit board to a chip loading substrate, and low-cost-ization of a semiconductor device can be attained together with using low melting point solder for a conductive member.
[0154] (4) -- between a . chip-substrate -- setting -- conductivity -- when a big load is applied to a semiconductor chip at the time of a mould by forming the gap section with the same narrow interval in the circumference of a member with the resin inflow prevention gap section, it can prevent that curvature which forms a crack in the principal plane of a semiconductor chip occurs Thereby, improvement in the reliability of a semiconductor device can be aimed at.
[0155] (5) By preparing the breakthrough which penetrates the aforementioned gap section and the exterior to . chip loading substrate, the gas which occurs in the gap section at the time of the elevated-temperature addition at the time of a mould and semiconductor device mounting etc. can be missed outside through a breakthrough. Thereby, generating of the package crack in a semiconductor device can be reduced further.
[0156] (6) Since the tooth back of a semiconductor chip is not exposed by wearing the exposed surface of . semiconductor chip with the resin for closure, and forming the closure section, touching the tooth back of a semiconductor chip directly at the time of the characterization of a semiconductor device and mounting etc. is lost. Since it can reduce by this that external force is added to a semiconductor chip, generating of the faulty connection between a chip crack or a chip-substrate can be prevented. Consequently, improvement in the reliability of a semiconductor device can be aimed at.
[0157] (7) Since the handling of a semiconductor device becomes easy by carrying out the resin seal of the . semiconductor chip, the manufacturability can be improved.
[0158] (8) By applying the soldering paste of . low melting point solder on the substrate terminal of a chip loading substrate, the process which forms a solder bump on the surface electrode of a semiconductor chip can be deleted in a last process (semiconductor chip manufacturing process). It becomes unnecessary furnishing this only for bump formation for performing flip chip bonding of the semiconductor device of this invention, consequently low-cost-ization of a semiconductor device can be attained.
[0159] (9) By manufacturing a semiconductor device using the base substrate equipped with the chip loading substrate of . plurality, it becomes possible to manufacture many semiconductor devices from one base substrate, and, thereby, a semiconductor device can be manufactured efficiently. Consequently, the manufacturability of a semiconductor device can be improved.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] Especially this invention relates to the semiconductor device and its manufacture method of the flip chip bonding which realizes low-cost-izing and high-reliability about a semiconductor manufacturing technology.

[Translation done.]

PRIOR ART

[Description of the Prior Art] the technology explained below -- this invention -- research -- it faces completing, this invention person inquires, and the outline is as follows

[0003] In the semiconductor device which has the semiconductor chip in which semiconductor integrated circuits, such as memory, were formed, BGA (Ball Grid Array) is known as an example of structure which attains the miniaturization. Furthermore, in Above BGA, flip chip bonding is used as technology of attaining improvement in the speed of signal transduction.

[0004] This flip chip bonding makes the active side (principal plane) of a semiconductor chip counter with the chip loading side of a chip loading substrate, and mounts a semiconductor chip in a chip loading substrate in this state.

[0005] In addition, in case flip chip bonding of the semiconductor chip is carried out, the surface electrode of a semiconductor chip and the substrate terminal of a chip loading substrate are mainly electrically connected using conductive members, such as a bump.

[0006] In this case, with the reflow temperature at the time of mounting BGA in mounting substrates, such as a printed-circuit board, a bump's connection uses melting and the bump formed with high-melting point solder in many cases so that it may expand and a package crack (crack formed in the closure section) may not be caused.

[0007] Furthermore, in order to raise a bump's connection reliability, some which form a golden bump with big size by the galvanizing method are in the pad (surface electrode) of the aluminum of a semiconductor chip.

[0008] Here, BGA which performed flip chip bonding is indicated by JP,9-82756,A, JP,9-92685,A, JP,6-326211,A, JP,7-111278,A, and JP,9-64231,A, for example.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] It will be as follows if the effect acquired by the typical thing among invention indicated in this application is explained briefly.
[0151] (1) . semiconductor chip and a chip loading substrate form the resin inflow prevention gap section, and are arranged -- between a chip-substrate -- setting -- conductivity -- the gap section can be formed in the circumference of a member Thereby, when a conductive member tends to expand thermally at the time of the external terminal installation by the reflow, or mounting to the mounting substrate of a semiconductor device, a conductive member can spread in the gap section. therefore, conductivity -- the stress generated according to the thermal expansion of a member can be made to be able to ease, consequently generating of the package crack at the time of semiconductor device mounting can be prevented Thereby, improvement in the reliability of a semiconductor device can be aimed at.
[0152] (2) Since generating of the package crack of . semiconductor device can be prevented, it can also be prevented the connectability between chip-substrates deteriorating.
[0153] (3) -- since a conductive member can expand thermally at the time of . semiconductor device mounting and it can spread in the gap section -- conductivity -- it becomes possible to be able to permit melting of a member, consequently to use low melting point solder for a conductive member Therefore, it becomes possible to use a comparatively cheap printed-circuit board to a chip loading substrate, and low-cost-ization of a semiconductor device can be attained together with using low melting point solder for a conductive member.
[0154] (4) -- between a . chip-substrate -- setting -- conductivity -- when a big load is applied to a semiconductor chip at the time of a mould by forming the gap section with the same narrow interval in the circumference of a member with the resin inflow prevention gap section, it can prevent that curvature which forms a crack in the principal plane of a semiconductor chip occurs Thereby, improvement in the reliability of a semiconductor device can be aimed at.
[0155] (5) By preparing the breakthrough which penetrates the aforementioned gap section and the exterior to . chip loading substrate, the gas which occurs in the gap section at the time of the elevated-temperature addition at the time of a mould and semiconductor device mounting etc. can be missed outside through a breakthrough. Thereby, generating of the package crack in a semiconductor device can be reduced further.
[0156] (6) Since the tooth back of a semiconductor chip is not exposed by wearing the exposed surface of . semiconductor chip with the resin for closure, and forming the closure section, touching the tooth back of a semiconductor chip directly at the time of the characterization of a semiconductor device and mounting etc. is lost. Since it can reduce by this that external force is added to a semiconductor chip, generating of the faulty connection between a chip crack or a chip-substrate can be prevented. Consequently, improvement in the reliability of a semiconductor device can be aimed at.
[0157] (7) Since the handling of a semiconductor device becomes easy by carrying out the resin seal of the . semiconductor chip, the manufacturability can be improved.
[0158] (8) By applying the soldering paste of . low melting point solder on the substrate terminal of a chip loading substrate, the process which forms a solder bump on the surface electrode of a semiconductor chip can be deleted in a last process (semiconductor chip manufacturing process). It becomes unnecessary furnishing this only for bump formation for performing flip chip bonding of the semiconductor device of this invention, consequently low-cost-ization of a semiconductor device can be attained.
[0159] (9) By manufacturing a semiconductor device using the base substrate equipped with the chip loading substrate of . plurality, it becomes possible to manufacture many semiconductor devices from one base substrate, and, thereby, a semiconductor device can be manufactured efficiently. Consequently, the manufacturability of a semiconductor device can be improved.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] however, in the flip chip bonding of said technology, when using high-melting point solder as a bump, you have to use the substrate which is high thermal resistance also for a chip loading substrate
[0010] Consequently, since high-melting point solder and the substrate of high thermal resistance are expensive, let it be a problem for BGA to carry out a cost rise.
[0011] Furthermore, since it is added like a plater to the manufacturing process of a semiconductor chip when forming a golden bump in the pad of a semiconductor chip by the galvanizing method, let it be a problem to introduce the facility for a plating application, consequently to lead to a cost rise like the above.
[0012] Moreover, in BGA indicated by said five official reports, in the structure, since the resin for closure is embedded to the circumference of the bump between the semiconductor chips and chip loading substrates by which flip chip bonding was carried out, melting and expanding (thermal expansion) and causing a package crack have a bump at the time of mounting of BGA.
[0013] Thereby, let it be a problem for the reliability of BGA to decrease.
[0014] The purpose of this invention is to offer the semiconductor device and its manufacture method of the flip chip bonding which realizes low-cost-izing and high-reliability.
[0015] The other purposes and the new feature will become clear from description and the accompanying drawing of this specification at the aforementioned row of this invention.

[Translation done.]

MEANS

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application.
[0017] Namely, the chip loading substrate to which the semiconductor device of this invention supports a semiconductor chip by flip chip bonding, The conductive member in which the surface electrode of the aforementioned semiconductor chip and the substrate terminal of the aforementioned chip loading substrate were electrically connected to, and the connection with the aforementioned surface electrode and the aforementioned substrate terminal was formed with low melting point solder, The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it, It is prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and has two or more external terminals electrically connected with the aforementioned substrate terminal. while the aforementioned semiconductor chip and the aforementioned chip loading substrate form the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and are arranged -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the gap section is formed in the circumference of a member
[0018] thereby -- conductivity -- since the gap section is formed in the circumference of a member -- conductivity -- the flexibility of a member is increased -- it can make -- consequently, conductivity -- the hindrance to the thermal expansion of a member can be reduced
[0019] therefore, the time of a conductive member carrying out thermal expansion (melting and expansion) at the time of mounting to the mounting substrate of a semiconductor device -- a conductive member -- the gap section -- it can spread -- thereby -- conductivity -- the stress generated according to the thermal expansion of a member can be made to ease
[0020] Consequently, generating of the package crack at the time of semiconductor device mounting can be prevented, and, thereby, improvement in the reliability of a semiconductor device can be aimed at.
[0021] Furthermore, the chip loading substrate to which the semiconductor device of this invention supports a semiconductor chip by flip chip bonding, The conductive member which connected electrically the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate, and was formed with low melting point solder, The closure section which was wearing the exposed surface of the aforementioned semiconductor chip with the resin for closure, and formed it, It is prepared in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side, and has two or more external terminals electrically connected with the aforementioned substrate terminal. while the aforementioned semiconductor chip and the aforementioned chip loading substrate form the resin inflow prevention gap section which prevents the inflow of the aforementioned resin for closure and are arranged -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- setting -- the aforementioned conductivity -- the gap section is formed in the circumference of a member
[0022] Moreover, the manufacture method of the semiconductor device of this invention makes the principal plane of a semiconductor chip, and the chip loading side of a chip loading substrate counter, and doubles the position of the surface electrode of the aforementioned semiconductor chip, and the substrate terminal of the aforementioned chip loading substrate corresponding to this. The process which arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through a conductive member between the aforementioned surface electrode and the aforementioned substrate terminal, The process which fuses the aforementioned conductive member, is made to connect the aforementioned surface electrode and the aforementioned substrate terminal electrically by the aforementioned conductive member where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate, the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member It has the process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, and the process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.
[0023] Furthermore, the process for which the chip loading substrate in which the substrate terminal corresponding to the surface electrode of a semiconductor chip in the manufacture method of the semiconductor device of this invention was prepared is prepared, The process which applies the soldering paste which consists of low melting point solder on the aforementioned substrate terminal of the aforementioned chip loading substrate, Make the principal plane of the aforementioned semiconductor chip, and the chip loading side of the aforementioned chip loading substrate counter, and the position of the aforementioned surface electrode and the aforementioned substrate terminal corresponding to this is doubled. The process which arranges the aforementioned semiconductor chip and the aforementioned chip loading substrate through the aforementioned soldering paste between the aforementioned surface electrode and the aforementioned substrate terminal, The aforementioned soldering paste is fused. The process which is electrically connected by the conductive member which formed the aforementioned surface electrode and the aforementioned substrate terminal from the aforementioned soldering

paste where the resin inflow prevention gap section is formed between the aforementioned semiconductor chip and the aforementioned chip loading substrate, and carries out flip chip bonding of the aforementioned semiconductor chip to the aforementioned chip loading substrate, the aforementioned resin inflow prevention gap section -- the inflow of the aforementioned resin for closure -- preventing -- between the aforementioned semiconductor chip and the aforementioned chip loading substrates -- the aforementioned conductivity, forming the gap section in the circumference of a member It has the process which is wearing the exposed surface of the aforementioned semiconductor chip and closes the aforementioned semiconductor chip with the aforementioned resin for closure, and the process which prepares two or more external terminals electrically connected with the aforementioned substrate terminal in the chip loading side of the aforementioned chip loading substrate, and the field of an opposite side.
[0024]
[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained in detail based on a drawing.

[0025] The perspective diagram which drawing 1 fractures a part of example of the structure of the semiconductor device (BGA) in the gestalt 1 of operation of this invention, and is shown, (Gestalt 1 of operation) Drawing 2 is drawing showing an example of the structure of BGA shown in drawing 1 . (a) A plan, The cross section with which an A-A line [in / drawing 2 (a) / (b) / a side elevation and (c), and / in drawing 3] is met, / a bottom plan view The expansion fragmentary sectional view showing the structure of the C section [in / drawing 3 / in drawing 4], the cross section with which drawing 5 meets the B-B line in drawing 2 (a), The manufacture process view showing an example of the manufacture method of a semiconductor device [in / the gestalt 1 of operation of this invention / in drawing 6] (BGA), Drawing 7 (a) and (b) The plan showing an example of the state of the base substrate in each manufacturing process of BGA shown in drawing 1 , The plan showing an example of the state of the base substrate in each manufacturing process of BGA which shows drawing 8 (a), (b), and (c) to drawing 1 , and the side elevation of BGA, Drawing 9 is the expansion fragmentary sectional view showing an example of the application state of the soldering paste in the manufacture method of BGA shown in drawing 1 . the conductivity in the manufacture method of BGA that (b) shows drawing 10 before a reflow to drawing 1 after a reflow in (a) -- the expansion fragmentary sectional view showing an example of the melting state at the time of the BGA mounting reflow of a member and drawing 11 are the physical-properties data views showing an example of the physical properties of the resin for closure used for BGA shown in drawing 1
[0026] The semiconductor device of the form 1 of this operation shown in drawing 1 - drawing 5 is BGA9 in which the semiconductor chip 1 by which semiconductor integrated circuits, such as memory (for example, SSRAM (Synchronous Static Random Access Memory)), were formed in principal plane 1b was mounted in the chip loading substrate 2 by flip chip bonding, and two or more solder balls 3 were formed as an external terminal.
[0027] In addition, the form 1 of this operation explains the case of BGA9 of 119 pins (7x17 pins) as an example of the above BGA 9. However, the number of external terminals, i.e., the number of installation of the solder ball 3, may not be limited to 119 pieces, and the number may be less than 119 pieces, or may be 119 or more pieces.
[0028] Moreover, in BGA9 explained with the form 1 of this operation, it is arranged in the shape of a grid (7x17), and is prepared in the field (henceforth referred to as substrate rear-face 2c) of chip loading side 2b and an opposite side in which land 2a (refer to drawing 4) whose solder ball 3 is the substrate terminal of the chip loading substrate 2 as shown in drawing 2 (b) and (c) is prepared.
[0029] Therefore, as shown in drawing 3 , the signal from a semiconductor chip 1 is told to the solder ball 3 which is an external terminal through the chip loading substrate 2.
[0030] The chip loading substrate 2 which will support a semiconductor chip 1 by flip chip bonding if the composition of the above BGA 9 is explained, the conductivity which connected electrically pad 1a (surface electrode) of a semiconductor chip 1, and land 2a of the chip loading substrate 2, and was formed with low melting point solder -- with a member 4 The closure section 6 which was wearing tooth-back 1c (exposed surface) of a semiconductor chip 1, and 1d (exposed surface) of sides with the resin 5 for closure, and formed them, Plurality which was prepared in substrate rear-face 2c of the chip loading substrate 2, and was electrically connected with land 2a (here) While it consists of 119 solder balls 3 which are external terminals, and a semiconductor chip 1 and the chip loading substrate 2 form the resin inflow prevention gap section 7 which prevents the inflow of the resin 5 for closure and are arranged between a semiconductor chip 1 and the chip loading substrates 2 (it omits between a chip-substrate henceforth) -- setting -- conductivity -- 2d of breakthroughs which the gap section 8 of the same interval is formed in the circumference of a member 4 with the resin inflow prevention gap section 7, and penetrate the gap section 8 and the exterior to the chip loading substrate 2 is prepared
[0031] 2d of this breakthrough is a vent hole for missing outside the gas which occurs in the gap section 8 at the time of a mould and a reflow etc.
[0032] Moreover, a semiconductor chip 1 is mounted in chip loading side 2b of the chip loading substrate 2 by flip chip bonding while it is formed with silicon.
[0033] in addition, as shown in drawing 1 , flip chip bonding is effective connection technology, when the size of a semiconductor chip 1 is comparatively large and it shortens connection distance between chip-substrates by this to the size of the appearance of BGA9 at the well of the case where application of wirebonding technology is difficult, and improvement in the speed of signal transduction
[0034] Drawing 4 is drawing having expanded and shown the structure of the flip-chip-bonding section of the gestalt 1 of this operation. Flip chip bonding makes the active side (principal plane 1b) of a semiconductor chip 1 counter with chip loading side 2b of the chip loading substrate 2, and mounts a semiconductor chip 1 in the chip loading substrate 2 in this state (face down).
[0035] in addition, pad 1a of a semiconductor chip 1 is formed by aluminum -- having -- a semiconductor chip 1 -- setting -- the upper layer of pad 1a -- conductivity -- barrier metal layer 1e electrically connected with connection 4a of a member 4 and 1f of protective coats which protect pad 1a are formed In that case, barrier metal layer 1e is formed of for example, a palladium-titanium alloy or a nickel chromium alloy, and exposes the front face, and is surrounded by 1f of protective coats, and, on the other hand, 1f of protective coats is formed of the insulator layer of for example, a polyimide system.
[0036] Furthermore, land 2a of the chip loading substrate 2 is formed for example, of the golden-copper alloy.

[0037] the conductivity which pad 1a of a semiconductor chip 1 and land 2a of the chip loading substrate 2 corresponding to this become from low melting point solder with the gestalt 1 of this operation here -- it connects directly electrically through the member 4 That is, it is the flip chip bonding by the eutectic-solder connection using low melting point solder.
[0038] In addition, the aforementioned low melting point solder is fused by the reflow at the temperature of 250 degrees C or less, and is low-temperature solder which is the grade which can be soldered.
[0039] Moreover, in case the aforementioned flip chip bonding is performed, thereby, a reflow of the soldering paste 10 (refer to drawing 9) applied to predetermined height by printing is carried out to land 2a of the chip loading substrate 2, or pad 1a of a semiconductor chip 1, the aforementioned soldering paste 10 is fused at once, it is made to harden and flip chip bonding is performed after that.
[0040] Consequently, the resin inflow prevention gap section 7 of an almost uniform request distance is formed over the whole periphery between chip-substrates.
[0041] This resin inflow prevention gap section 7 is the crevice formed so that the resin 5 for closure might not enter between chip-substrates at the time of a resin seal, and is formed in the grade which can prevent the inflow of the resin 5 for closure at the time of a resin seal very narrowly.
[0042] Moreover, the closure section 6 of BGA9 of the gestalt 1 of this operation is formed of the transfermold which used the resin 5 for closure among resin seals.
[0043] Therefore, the set point of the distance of the aforementioned resin inflow prevention gap section 7 is determined by the physical properties of the resin 5 for closure used with the gestalt 1 of this operation shown in drawing 11 , and the mould conditions at the time of the mould mentioned later, and, in the case of the gestalt 1 of this operation, the distance of the resin inflow prevention gap section 7 is about 20 micrometers as the example.
[0044] However, if the value of the distance of the resin inflow prevention gap section 7 is the size which can prevent the inflow of a between [the chip-substrates of the resin 5 for closure at the time of a resin seal], it is not limited to 20 micrometers and can be variously changed according to combination, its kind, etc. of the resin 5 (for example, fluidity) for closure to be used, and mould conditions at the time of a mould.
[0045] In addition, since the resin 5 for closure does not flow between chip-substrates in the above BGA 9 as described above, in case the resin seal of the semiconductor chip 1 is carried out by the mould method, each conductivity which consists of low melting point solder -- the gap section 8 is formed in the circumference of a member 4, and the resin inflow prevention gap section 7 formed over the whole periphery between chip-substrates and the gap section 8 of the inner direction between chip-substrates are formed in the same distance in BGA9 of the gestalt 1 of this operation
[0046] That is, principal plane 1b of a semiconductor chip 1 and chip loading side 2b of the chip loading substrate 2 are mutually formed of a flat field, and thereby, it is formed so that the distance between chip-substrates may be mostly set to about 20 micrometers from 1g of periphery sections of a semiconductor chip 1 over the whole inner one at homogeneity.
[0047] moreover, between a chip-substrate -- setting -- each conductivity -- a semiconductor chip 1 can consider curving slightly in the sense by which the circuit forming face (principal plane 1b) is pulled by having formed the gap section 8 in the circumference of a member 4 This amount of curvatures of a semiconductor chip 1 must be the amount of curvatures of the grade which does not form a crack in principal plane 1b of a semiconductor chip 1 in that case.
[0048] In the gap section 8 during installation of a member 4 therefore, two or more conductivity which supports a semiconductor chip 1 -- the conductivity which adjoins among members 4 -- two conductivity from which the installation pitch of a member 4 serves as the maximum -- Having to consider the size of the gap section 8 as it being possible to stop in the amount of curvatures of the grade which does not form a crack in the principal plane 1b, when a semiconductor chip 1 curves, the 20-micrometer gap section 8 in the gestalt 1 of this operation satisfies this condition.
[0049] Moreover, using the resin 5 for closure, the closure section 6 of the above BGA 9 closes a semiconductor chip 1 by transfermold, and is formed, and as shown in drawing 1 and drawing 2 (a), the resin 5 for closure near the circumference of a semiconductor chip 1 in the chip loading substrate 2 are joined over the perimeter almost in accordance with 1d of four sides of a semiconductor chip 1.
[0050] In addition, the resin 5 for closure shows the physical properties of the resin 5 for closure used in the gestalt 1 of this operation as the example to drawing 11 , although it is a thermosetting epoxy system resin etc.
[0051] Moreover, the chip loading substrate 2 is a printed-circuit board of plastics with the comparatively cheap and moderate thermal resistance (not a high heatproof but thermal resistance for example, around 300 degrees C) formed using for example, the epoxy system resin containing glass, the bismaleimide triazine containing glass (BT resin containing glass), etc.
[0052] Therefore, BGA9 of the gestalt 1 of this operation is called P-BGA (plastics BGA).
[0053] Moreover, as shown in drawing 3 , the chip loading substrate 2 is a substrate of the multilayer-interconnection structure where 2f of front wiring and 2g of internal wiring were formed, while the front face is coated with solder-resist 2e, as shown in drawing 5 . The chip loading substrate 2 of the gestalt 1 of this operation is a substrate of four layer structures with four wiring layers in 2f of front wiring of chip loading side 2b, the front wiring of 2f of substrate rear-face 2c, and 2g of two internal wiring, as shown in drawing 3 .
[0054] However, the chip loading substrate 2 is not limited to the substrate of four layer structures.
[0055] Furthermore, 2d of one breakthrough of a vent-hole function is formed in the part which avoided land 2a near the center of chip loading side 2b. However, also about the number of installation of 2d of breakthroughs, it may not be limited and more than one may be prepared.
[0056] moreover, the solder ball 3 which is the external terminal of BGA9 -- conductivity -- it is formed with low melting point solder like a member 4, and the size is about 0.75mm in diameter
[0057] Next, the manufacture method of the semiconductor device (BGA) by the gestalt 1 of this operation is explained.
[0058] In addition, the manufacture method of the aforementioned semiconductor device is two or more sheets (here, although the case of six sheets is explained as the example) which are the manufacture methods of BGA9 shown in drawing 1 - drawing 5 , and are shown in drawing 7 and drawing 8 with the gestalt 1 of this operation. Based on the manufacture process which shows the case where BGA9 of plurality (six pieces) is manufactured to drawing 6 , it explains from one base substrate 11 equipped with chip loading substrates 2 of being two or more sheets other than six sheet.

[0059] First, by Step S1 shown in drawing 6 , the dicing which prepares a semiconductor wafer (not shown) equipped with two or more semiconductor chips 1 in which the desired semiconductor integrated circuit was formed, then is shown in Step S2 is performed, and the aforementioned semiconductor wafer is cut and separated at each semiconductor chip 1.
[0060] Then, the semiconductor chip 1 judged by inspection etc. to be an excellent article is prepared, and the base substrate 11 further equipped with six chip loading substrates 2 in which substrate terminal 2a corresponding to pad 1a of this semiconductor chip 1 was prepared is prepared.
[0061] Here, the base substrate 11 is a large-sized substrate which arranged the aforementioned BGA field in one train continuously while forming six pieces of the chip loading substrate 2 equivalent to one BGA field in one, as shown in drawing 7 (a).
[0062] Moreover, two or more tooling-holes 11a and guide long hole 11b which are used for this base substrate 11 at the time of a mould or cutting etc. are respectively prepared in the both-sides section along with the longitudinal direction of the base substrate 11 corresponding to each chip loading substrate 2.
[0063] That is, the base substrate 11 is a substrate which took and **(ed) six chip loading substrates 2.
[0064] Then, while performing base substrate supply shown in Step S3, soldering paste supply shown in step S4 is performed, and soldering paste printing shown in Step S5 to substrate terminal 2a of each chip loading substrate 2 of the base substrate 11 is performed.
[0065] the soldering paste 10 which consists of low melting point solder shown in drawing 9 (a) with the gestalt 1 of this operation here in case the aforementioned soldering paste printing is performed -- a mask -- it carries out to predetermined height by carrying out a printing application on substrate terminal 2a of the chip loading substrate 2 using a member 12 (height control-section material)
[0066] in addition, a mask -- a member 12 is a member for carrying out the printing application of the soldering paste 10 at height highly precise on substrate terminal 2a
[0067] With the gestalt 1 of this operation, the resin inflow prevention gap section 7 and the gap section 8 are formed in about 20 micrometers. as an example of a method which realizes this -- a mask -- the time of forming the soldering paste 10 of low melting point solder on substrate terminal 2a by the member 12 -- the diameter of 40 micrometers -- and soldering paste 10 is formed with a precision sufficient to a cylindrical shape with a height of 100 micrometers
[0068] namely, the diameter of 40 micrometers -- and the soldering paste 10 of a cylindrical shape with a height of 100 micrometers -- it should form -- opening -- a mask -- it is formed in the member 12
[0069] If the soldering paste 10 in which this height and size were controlled with high precision, and were formed on substrate terminal 2a is fused by the reflow and stiffened after that, as shown in drawing 9 (b), the resin inflow prevention gap section 7 and the gap section 8 can be formed in about 20 micrometers.
[0070] In addition, the connection reliability between chip-substrates can be improved by making the printing (application) height of soldering paste 10 as low as possible. However, the size or configuration of soldering paste 10 which are printed on substrate terminal 2a are not determined by the distance of the resin inflow prevention gap section 7 and the gap section 8 etc., and neither the aforementioned size nor a configuration (the form 1 of this operation the diameter of 40 micrometers and cylindrical shape with a height of 100 micrometers) is limited to this in that case.
[0071] a mask -- on the base substrate 11 by the aforementioned printing method using the member 12, after carrying out the printing application of the soldering paste 10 on predetermined substrate terminal 2a of the chip loading substrate 2 at predetermined height Principal plane 1b of six semiconductor chips 1 and chip loading side 2b of the chip loading substrate 2 corresponding to each are made to counter. And the position of pad 1a of each semiconductor chip 1 and substrate terminal 2a corresponding to this is doubled, and a semiconductor chip 1 and the chip loading substrate 2 are further arranged through soldering paste 10 between pad 1a and substrate terminal 2a.
[0072] That is, chip mounting shown in Step S6 using the chip mounter for the existing flip chip bonding etc. is performed.
[0073] The base substrate 11 shown in drawing 7 (b) shows the state where chip mounting of the six semiconductor chips 1 was carried out to each BGA field.
[0074] Then, through and this perform the reflow shown in Step S7 at the reflow furnace which does not illustrate the base substrate [finishing / chip mounting] 11 shown in drawing 7 (b).
[0075] That is, by the aforementioned reflow, soldering paste 10 is fused and, thereby, between a chip-substrate is connected electrically.
[0076] consequently, the conductivity which formed pad 1a and substrate terminal 2a from soldering paste 10 where the resin inflow prevention gap section 7 is formed between six semiconductor chips 1 and the chip loading substrate 2 corresponding to these -- by the member 4, it can be made to connect electrically and, thereby, flip chip bonding of each semiconductor chip 1 is carried out to each chip loading substrate 2
[0077] In addition, the reflow temperature at the time of a reflow is 240-250 degrees C.
[0078] Here, soldering paste 10 is the height and size (here). Since a cylindrical shape with a diameter [of 40 micrometers] and a height of 100 micrometers is controlled with high precision and applied, the aforementioned reflow -- soldering paste 10 -- once -- fusing -- after that -- getting cold -- hardening -- conductivity -- if it becomes a member 4, as shown in drawing 4 and drawing 9 (b), the distance of the distance 7 of a semiconductor chip 1 and the chip loading substrate 2, i.e., the resin inflow prevention gap section, and the gap section 8 will be set to 20 micrometers
[0079] Resin supply for closure which supplies this is performed after a reflow end using the resin 5 for closure of the physical properties shown in drawing 11 (Step S8), and the resin seal of a semiconductor chip 1 is performed (Step S9).
[0080] In addition, in the form 1 of this operation, transfermold performs a resin seal.
[0081] Moreover, with the form 1 of this operation, the mould conditions at the time of performing a mould, the physical properties of the resin 5 for closure, and the distance of the resin inflow prevention gap section 7 become an important factor for not making the resin 5 for closure permeate between chip-substrates at the time of a mould.
[0082] Then, when the distance of the resin inflow prevention gap section 7 is set up with about 20 micrometers, while the resin 5 for closure which cannot permeate between chip-substrates is a resin which has the physical properties shown in drawing 11 , the mould conditions for not making the resin 5 for closure permeate between chip-substrates at the time of a mould are the things of the following contents.

[0083] the mould which does not illustrate the aforementioned mould conditions -- metal mold -- the plunger pressure which is a pressure when extruding the resin 5 for closure inside -- 150 kg/cm2 and a mould -- in MAX, the speed [t / 50] at which the clamp pressure (mold-clamp pressure) of metal mold flows, and 175 degrees C and the resin 5 for closure flow / a die temperature / is 1.62 mm/sec, and mould time is 220 seconds
[0084] Therefore, if the aforementioned mould conditions perform transfermold, using the resin 5 for closure which has the physical properties shown in drawing 11 in order that the 20-micrometer resin inflow prevention gap section 7 may prevent the inflow of a between [the chip-substrates of the resin 5 for closure] and the resin 5 for closure may not permeate between chip-substrates by this -- between each semiconductor chip 1 and the chip loading substrates 2 -- conductivity -- the gap section 8 can be formed in the circumference of a member 4
[0085] consequently, between a chip-substrate -- conductivity -- with the structure which formed the gap section 8 in the circumference of a member 4, tooth-back 1c of each semiconductor chip 1 and 1d of sides are worn with the resin 5 for closure, six semiconductor chips 1 are boiled, respectively, are closed, and the closure section 6 is formed
[0086] In addition, in the resin seal of the form 1 of this operation, the resin 5 for closure is supplied to the exposed surface of a semiconductor chip 1, i.e., tooth-back 1c, and 1d of sides, a semiconductor chip 1 is completely covered with the resin 5 for closure on the chip loading substrate 2, and the closure section 6 is formed.
[0087] This forms BGA book soma 9a (semiconductor device book soma) containing the six closure sections 6 on one base substrate 11, as shown in drawing 8 (a).
[0088] Then, six BGA book soma 9a is cut, respectively, and it is made to dissociate from the base substrate 11, as shown in drawing 8 (b) (Step S10).
[0089] As a cutting process in that case, a router (drill) may be used and mold cutting etc. may cut.
[0090] Then, the solder ball 3 which is the external terminal of plurality (the form 1 of this operation 119 pieces) electrically connected with substrate terminal 2a, and is set to the field of chip loading side 2b and an opposite side, i.e., substrate rear-face 2c, in the chip loading substrate 2 of each BGA book soma 9a from low melting point solder is formed.
[0091] Here, first, solder ball supply (Step S11) is performed, the solder ball imprint shown in Step S12 is performed further, and temporary fixation of the 119 solder balls 3 is carried out at the chip loading substrate 2 of each BGA book soma 9a.
[0092] Then, through and this perform the reflow shown in Step S13 at the reflow furnace which does not illustrate the base substrate 11 which carried out temporary fixation of the solder ball 3 to each chip loading substrate 2.
[0093] That is, the solder ball 3 is attached in the chip loading substrate 2 by the reflow shown in Step S13.
[0094] In addition, the reflow temperature at the time of a reflow is 240-250 degrees C.
[0095] here -- conductivity -- since a member 4 is formed from the soldering paste 10 of low melting point solder, it is shown in drawing 10 at the time of a 240-250-degree C reflow -- as -- each conductivity -- it fuses, and a member 4 expands thermally and spreads in a longitudinal direction
[0096] this time -- BGA9 of the form 1 of this operation -- each conductivity -- since the gap section 8 is formed in the circumference of a member 4 -- conductivity -- the increase of flexibility, consequently conductivity of a member 4 -- a member 4 can be spread and shortened in the gap section 8
[0097] Thereby, the solder ball 3 which is the external terminal which consists of low melting point solder is attached.
[0098] Consequently, BGA9 as shown in drawing 1 or drawing 8 (c) can be manufactured, and, thereby, it can consider as BGA completion (Step S14).
[0099] According to the semiconductor device (BGA) and its manufacture method of a form 1 of this operation, the following operation effects are acquired.
[0100] That is, the inflow of the resin 5 for closure of a between [the chip-substrate at the time of a mould (at the time of a resin seal)] can be prevented by a semiconductor chip 1 and the chip loading substrate 2 forming the resin inflow prevention gap section 7, and arranging them.
[0101] therefore, between the aforementioned chip-substrate -- setting -- conductivity -- the gap section 8 can be formed in the circumference of a member 4
[0102] thereby -- conductivity -- since the gap section 8 is formed in the circumference of a member 4 -- conductivity -- the flexibility of a member 4 is increased -- it can make -- consequently, conductivity -- the hindrance to the thermal expansion and cooling of a member 4 can be reduced
[0103] therefore, the time of mounting to mounting substrates, such as a printed circuit board of the time of the solder ball 3 (external terminal) installation by the reflow, or BGA9, -- conductivity -- the time of a member 4 carrying out thermal expansion (melting and expansion) -- conductivity -- a member 4 can spread in the gap section 8, and it can also be shortened when it got cold and hardens
[0104] thereby -- conductivity -- the stress generated according to the thermal expansion (cooling) of a member 4 can be made to ease
[0105] Consequently, generating of the package crack at the time of BGA9 mounting can be prevented, and, thereby, improvement in the reliability of BGA9 can be aimed at.
[0106] Furthermore, it can also be prevented the connectability between chip-substrates deteriorating.
[0107] moreover, the time of BGA9 mounting -- conductivity -- since a member 4 can expand thermally and it can spread in the gap section 8 -- conductivity -- melting of a member 4 -- being permissible -- consequently, conductivity -- it becomes possible to use low melting point solder for a member 4
[0108] therefore, the thing for which a printed-circuit board with the thermal resistance which it is comparatively cheap and is not a high heatproof is used to the chip loading substrate 2 -- possible -- becoming -- conductivity -- low-cost-ization of BGA9 can be attained together with using low melting point solder for a member 4
[0109] moreover, between a chip-substrate -- setting -- conductivity -- since this gap section 8 is about about 20 micrometers by forming the gap section 8 of the same interval in the circumference of a member 4 with the resin inflow prevention gap section 7, when a big load is applied to a semiconductor chip 1 at the time of a mould, it can prevent that curvature which forms a crack in principal plane 1b of a semiconductor chip 1 occurs
[0110] Thereby, improvement in the reliability of BGA9 can be aimed at.
[0111] Furthermore, the gas which occurs in the gap section 8 at the time of the elevated-temperature addition at the time of

a mould and BGA9 mounting etc. can be missed outside through 2d of breakthroughs by preparing 2d of breakthroughs which penetrate the gap section 8 and the exterior to the chip loading substrate 2.
[0112] Thereby, generating of the package crack in BGA9 can be reduced further.
[0113] Moreover, since principal plane 1b and tooth-back 1c of a semiconductor chip 1 are not exposed by wearing tooth-back 1c and 1d of sides which are an exposed surface of a semiconductor chip 1 with the resin 5 for closure, and forming the closure section 6, touching tooth-back 1c of a semiconductor chip 1 directly at the time of the characterization of BGA9 and mounting etc. is lost.
[0114] Since it can reduce by this that external force is added to a semiconductor chip 1, generating of the faulty connection between a chip crack or a chip-substrate can be prevented.
[0115] Consequently, improvement in the reliability of BGA9 can be aimed at.
[0116] Furthermore, since the handling of BGA9 becomes easy by carrying out the resin seal of the semiconductor chip 1, the manufacturability can be improved.
[0117] Moreover, by applying the soldering paste 10 of low melting point solder on substrate terminal 2a of the chip loading substrate 2, in a last process (manufacturing process of a semiconductor chip 1), the process which forms a solder bump on pad 1a of a semiconductor chip 1 can be deleted, and it becomes possible to consider as the same last process as the semiconductor chip 1 which does not perform flip chip bonding by this.
[0118] Therefore, since the facility only for bump formation for performing flip chip bonding of BGA9 of the form 1 of this operation becomes unnecessary consequently, low-cost-ization of BGA9 can be attained.
[0119] Moreover, by manufacturing BGA9 using the base substrate 11 equipped with six chip loading substrates 2, it becomes possible to manufacture six BGA9 simultaneously from one base substrate 11, and, thereby, BGA9 can be manufactured efficiently. That is, the throughput in the manufacturing process of BGA9 can be improved.
[0120] Consequently, the manufacturability of BGA9 can be improved.
[0121] (Form 2 of operation) the conductivity prepared in the semiconductor chip of BGA which shows the cross section showing an example of the structure of a semiconductor device [in / the form 2 of operation of this invention / in drawing 12] (BGA), the expansion fragmentary sectional view showing the structure of the D section / in / drawing 12 / in drawing 13], and drawing 14 to drawing 12 -- it is the bottom plan view showing an example of the array of a member
[0122] Although BGA20 (semiconductor device) shown in drawing 12 in the form 2 of this operation mounts a semiconductor chip 1 in the chip loading substrate 2 by flip chip bonding like BGA9 explained with the form 1 of operation and it has the almost same structure as BGA9 The change part over BGA9 of the form 1 of operation it is shown in drawing 13 -- as -- conductivity -- it is with using the small solder ball which becomes a member 4 from low melting point solder, and forming only in the part corresponding to 1g of periphery sections of the semiconductor chip 1 of the chip loading substrate 2 the resin inflow prevention gap section 7 which prevents the inflow of the resin 5 for closure
[0123] therefore, BGA20 -- the conductivity of the aforementioned small solder ball -- flip chip bonding of the semiconductor chip 1 is carried out to the chip loading substrate 2 through a member 4
[0124] the form 2 of this operation here -- conductivity -- the size of the aforementioned small solder ball used as a member 4 is about 0.2mm in diameter
[0125] Thereby, when flip chip bonding of the semiconductor chip 1 is carried out to the chip loading substrate 2 by the reflow etc., the distance of the gap section 8 between chip-substrates turns into distance of a grade [a little] shorter than 0.2mm.
[0126] Therefore, the 20-micrometer resin inflow prevention gap section 7 is formed only in the part corresponding to 1g of periphery sections of the semiconductor chip 1 of the chip loading substrate 2 at the time of carrying a semiconductor chip 1 in the chip loading substrate 2.
[0127] That is, as shown in drawing 13 , 2h of dam sections of the letter of a salient which consists of solder-resist 2e is prepared in the part corresponding to 1g perimeter of periphery sections of the semiconductor chip 1 of the chip loading substrate 2, and this realizes formation of the 20-micrometer resin inflow prevention gap section 7.
[0128] the conductivity of the small solder ball of the form 2 of this operation here -- in case a member 4 performs flip chip bonding, beforehand, it is carried in the pad 1a side of a semiconductor chip 1, and a face down carries out flip chip mounting (chip mounting) of the semiconductor chip 1 which carried this small solder ball to the chip loading substrate 2
[0129] In addition, the distance of the gap section 8 in BGA20 of the form 2 of this operation is the distance of a grade short a little, and is longer than 0.2mm to ** compared with 20 micrometers of BGA9 of the form 1 of operation.
[0130] Therefore, in case transfermold performs a resin seal, we are anxious about a semiconductor chip 1 curving according to a mould load, and being divided.
[0131] however, by BGA20 of the form 2 of this operation, in order to reduce the curvature of the semiconductor chip 1 at the time of a mould, it is shown in drawing 14 -- as -- the conductivity of the small solder ball of plurality (here about 140 pieces) -- the member 4 is attached in the semiconductor chip 1 in the grid-like array
[0132] In addition, in case the aforementioned grid-like array is performed, when the number of the aforementioned small solder balls is insufficient, the dummy bump who is not making electric connection between chip-substrates is attached, and a grid-like array is prepared.
[0133] Since it is the same as that of BGA9 explained with the form 1 of operation about the structure of others in BGA20 of the form 2 of this operation here, the duplication explanation is omitted.
[0134] Moreover, at BGA20 of the form 2 of this operation, it is stud bump technology to the difference with the form 1 of operation having applied soldering paste 10 to the chip loading substrate 2 side in BGA9 of the form 1 of operation, although the manufacture method of BGA20 of the form 2 this operation was almost the same as the manufacture method of BGA9 of the form 1 operation, and having performed flip chip bonding.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the perspective diagram fracturing and showing a part of example of the structure of the semiconductor device (BGA) in the gestalt 1 of operation of this invention.
[Drawing 2] (a), (b), and (c) are drawings showing an example of the structure of BGA shown in drawing 1 , and (a) is [a side elevation and (c of a plan and (b))] bottom plan views.
[Drawing 3] It is the cross section which meets the A-A line in drawing 2 (a).
[Drawing 4] It is the expansion fragmentary sectional view showing the structure of the C section in drawing 3 .
[Drawing 5] It is the cross section which meets the B-B line in drawing 2 (a).
[Drawing 6] It is the manufacture process view showing an example of the manufacture method of the semiconductor device (BGA) in the gestalt 1 of operation of this invention.
[Drawing 7] (a) and (b) It is the plan showing an example of the state of the base substrate in each manufacturing process of BGA shown in drawing 1 .
[Drawing 8] (a), (b), and (c) are the plans and the side elevations of BGA showing an example of the state of the base substrate in each manufacturing process of BGA shown in drawing 1 .
[Drawing 9] (a) and (b) It is the expansion fragmentary sectional view showing an example of the application state of the soldering paste in the manufacture method of BGA shown in drawing 1 , and (a) is before a reflow and (b) is after a reflow.
[Drawing 10] the conductivity in the manufacture method of BGA shown in drawing 1 -- it is the expansion fragmentary sectional view showing an example of the melting state at the time of the BGA mounting reflow of a member
[Drawing 11] It is the physical-properties data view showing an example of the physical properties of the resin for closure used for BGA shown in drawing 1 .
[Drawing 12] It is the cross section showing an example of the structure of the semiconductor device (BGA) in the gestalt 2 of operation of this invention.
[Drawing 13] It is the expansion fragmentary sectional view showing the structure of the D section in drawing 12 .
[Drawing 14] the conductivity prepared in the semiconductor chip of BGA shown in drawing 12 -- it is the bottom plan view showing an example of the array of a member
[Description of Notations]
1 Semiconductor Chip
1a pad (surface electrode)
1b Principal plane
1c Tooth back (exposed surface)
1d Side (exposed surface)
1e Barrier metal layer
1f Protective coat
1g Periphery section
2 Chip Loading Substrate
2a Land (substrate terminal)
2b Chip loading side
2c Substrate rear face
2d Breakthrough
2e Solder resist
2f Front wiring
2g Internal wiring
2h Dam section
3 Solder Ball (External Terminal)
4 Conductivity -- Member
4a Connection
5 Resin for Closure
6 Closure Section
7 Resin Inflow Prevention Gap Section
8 Gap Section
9 BGA (Semiconductor Device)
9a BGA book soma (semiconductor device book soma)
10 Soldering Paste
11 Base Substrate
11a Tooling holes
11b Guide long hole
12 Mask Member (Height Control-Section Material)

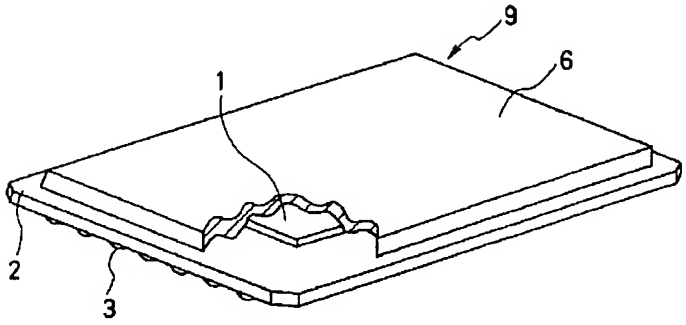
20 BGA (Semiconductor Device)

[Translation done.]

DRAWINGS

[Drawing 1]

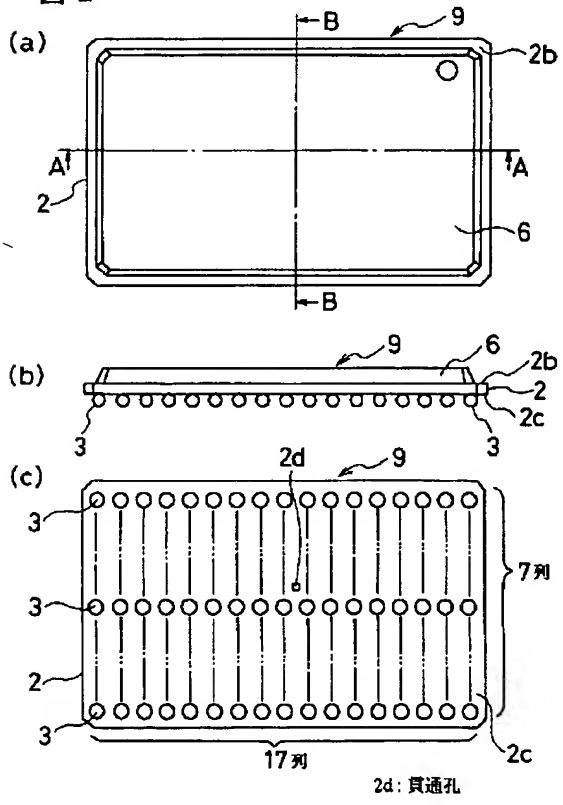
図 1



3：はんだボール(外部端子)
6：封止部
9：BGA(半導体装置)

[Drawing 2]

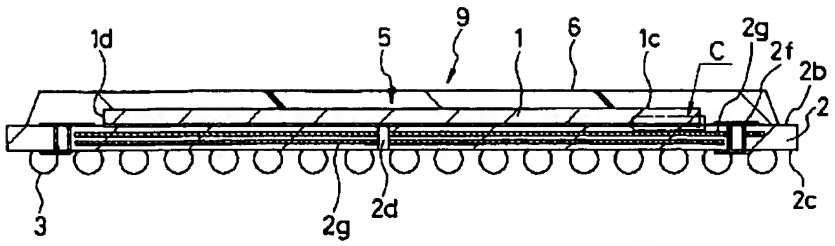
図 2



2d：貫通孔

[Drawing 3]

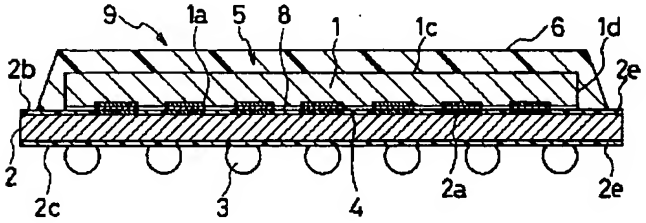
図 3



1c：背面(露出面)
1d：側面(露出面)
5：封止用樹脂

[Drawing 5]

図 5



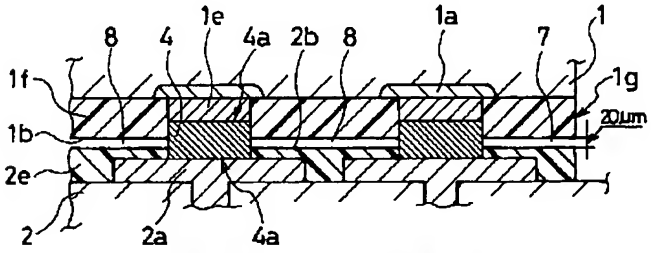
[Drawing 11]

図 11

組成	エポキシ	———	ビフェニル
物性	Tg	℃	125±10
	α1	ppm/℃	12
	ヤング率	kg/mm²	2200
成形物性	スパイラルフロー	inch	30±4
	ゲルタイム(160℃)	sec	50±10
	バリ	mm	2.0↓

[Drawing 4]

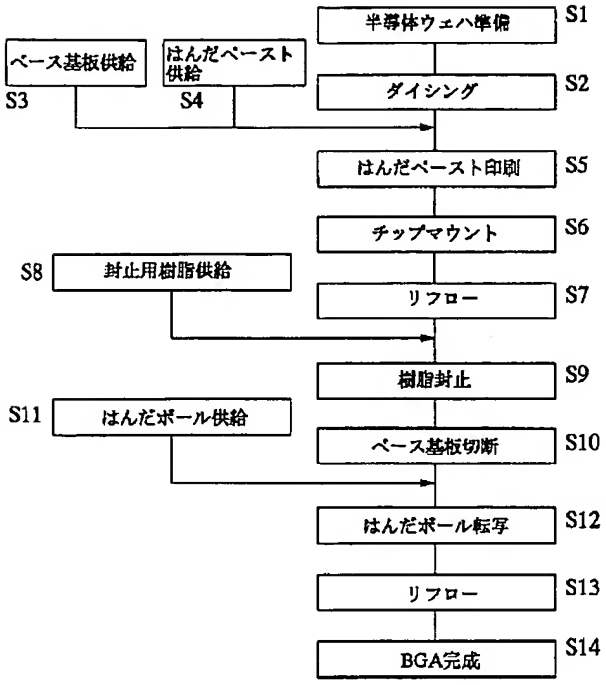
図 4



1：半導体チップ
1a：パッド(表面電極)
1b：主面
2：チップ搭載基板
2a：ランド(基板端子)
2b：チップ搭載面
4：導電性部材
4a：接続部
7：樹脂流入阻止溝部
8：間隙部

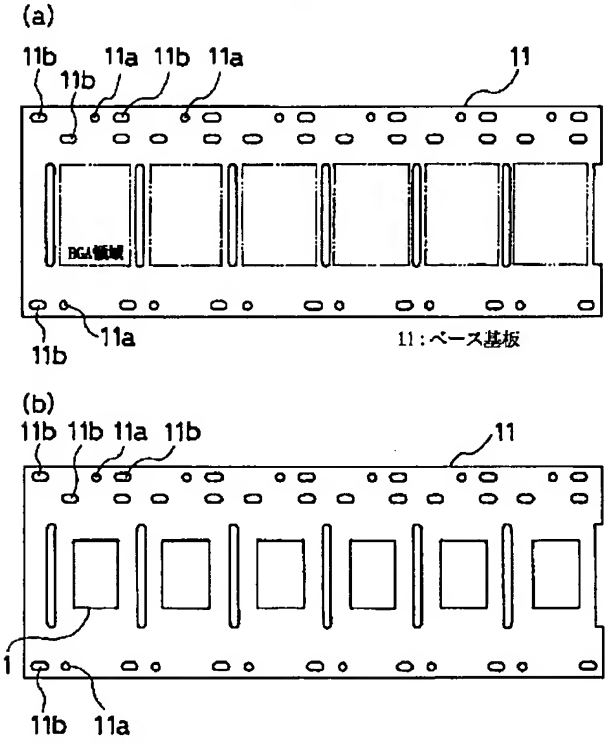
[Drawing 6]

図 6



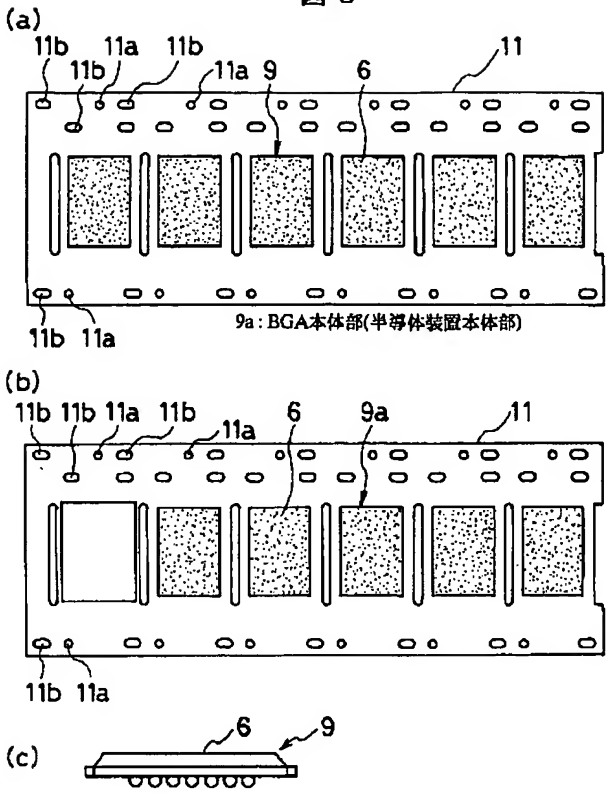
[Drawing 7]

図 7



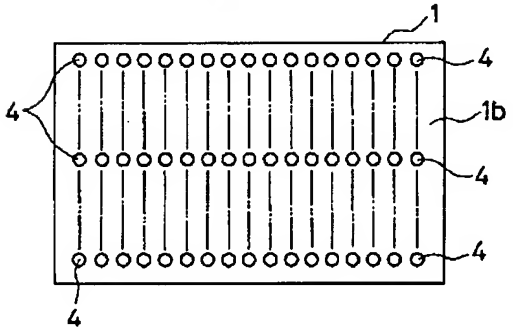
[Drawing 8]

図 8



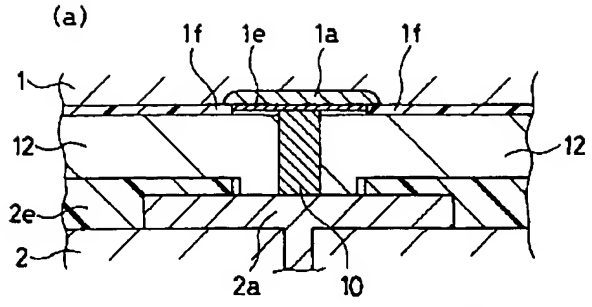
[Drawing 14]

図１４



[Drawing 9]

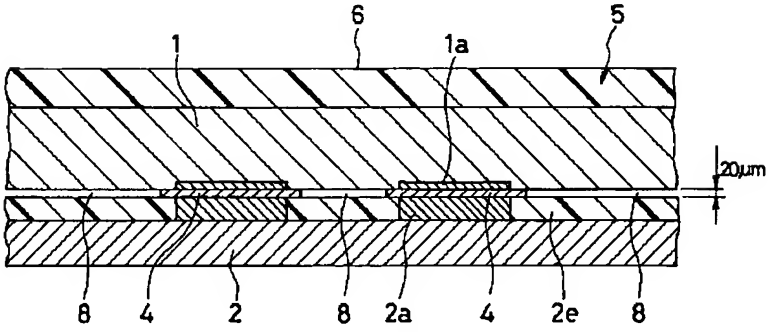
図 9



10：はんだペースト
12：マスク部材(高さ制御部材)

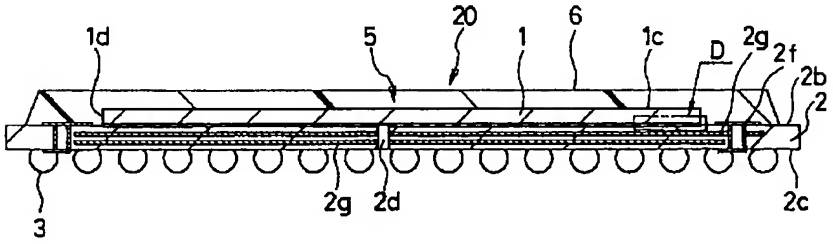
[Drawing 10]

図１０



[Drawing 12]

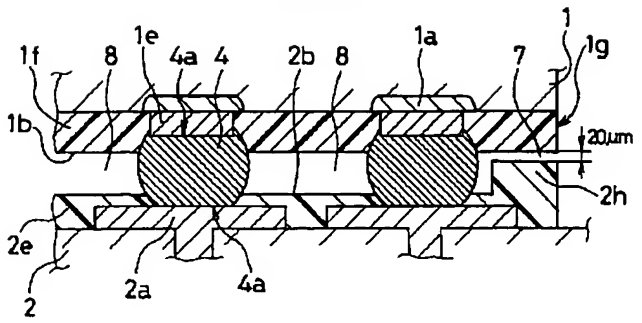
図１２



20：BGA(半導体装置)

[Drawing 13]

図１３



[Translation done.]